



2001 *International*

INTEGRATED RELIABILITY WORKSHOP



October 15-18, 2001

<http://www.irps.org/irw/>

Stanford Sierra Camp, Lake Tahoe, CA

CALL FOR PAPERS

The Integrated Reliability Workshop continues to focus on ensuring semiconductor reliability through component fabrication, design, characterization, and analysis tools. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. The workshop provides a forum for presentations, posters, topical discussion groups and issue-focused special interest groups.

Hot reliability topics of the workshop are: Cu interconnects, reliability of deep sub-micron, high-speed, high-frequency devices (e.g. SiGe), SOI devices, product reliability, burn-in techniques, negative bias temperature device instability, soft errors, new dielectric systems, and reliability modeling & simulation.

We invite you to submit a presentation proposal that addresses one or more of the following topics:

● **WAFER LEVEL RELIABILITY TESTS AND**

TEST APPROACHES:

fast stress tests and analysis methodologies, reduction in development time, in-line monitors, relation to circuit-element and package-level tests, use and interpretation of WLR data; success stories; the fine tuning of a WLR implementation.

● **IDENTIFICATION OF RELIABILITY EFFECTS:**

failure mechanisms and sensitivities to materials and manufacturing; new reliability aspects of: novel dielectric systems, Cu interconnects, MOS and bipolar transistors, and MEMS devices.

● **NEW OR EXISTING RELIABILITY CHARACTERIZATION AND PREDICTION MODELS TO SHOW:**

limits to accelerated stress, (non-) correlation of short- and long-duration stress results, applications for AC, pulsed, and DC conditions.

● **RELIABILITY TEST STRUCTURES:**

design, characterization, uses, and data analysis; for chip or package level (including electrical and/or physical test/analysis).

● **CUSTOMER PRODUCT RELIABILITY REQUIREMENTS/**

MANUFACTURER RELIABILITY TASKS:

future reliability targets, reliability evaluation methodologies; reporting systems; databases, burn-in strategy, soft error rate analysis.

● **DESIGNING-IN RELIABILITY**

(CIRCUITS, PROCESSES, PRODUCTS):

methodologies and concepts, modeling, simulation tools, reliability-driven design rules and checkers; use of WLR for design rule verification.

SUBMISSION DEADLINE: *Received no later than July 6, 2001.*

Your submission should state clearly and concisely the results of your work and why they are significant. Representative data and/or figures that support your proposal are REQUIRED. We accept both oral presentation and poster submissions. Please state which submission category you prefer. Oral presentations require preparation of a paper for the Final Report. Poster presenters may also submit written material for the Final Report.

Please e-mail your two-page (maximum) abstract (incl. figures) as an MS Word document or pdf file. Or, you may airmail (express mail preferred) your abstract to the Technical Program Chair. Your proposal must include the name, affiliation, complete return address, telephone and telefax numbers, and e-mail address for each author. Telefax submissions will NOT be accepted. All submissions will be acknowledged within three weeks. Please contact the Technical Program Chair if you do not hear from us.

Visual aids for the ACCEPTED paper proposals are required by September 17, 2001 for inclusion in the Presentation Handout available at the workshop. A written version of your presentation is due at the workshop for inclusion in the Final Report.

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