IEEE/Integrated Reliability Workshop
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Harry Schafft, NIST
Andreas Martin, Infineon

PROGRAM ANNOUNCEMENT!

Workshop Experience

You are cordially invited to participate in the 2002 Integrated Reliability Workshop. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. Here you will closely interact with your peers at moderated discussion groups, open poster sessions, technical presentations, and special interest groups. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learning and knowledge sharing. You will come away from the workshop intellectually refreshed!

'02 Workshop Features:

- **Keynote:** ***"Embedded Non-Volatile Memory Qualification Methodologies for Automotive Applications,"*** **John Bridwell, Manager, Reliability & Device Analysis, Motorola Semiconductor Products Sector**
- **Group Discussions**
  - **Electromigration**
  - **Ultra-thin Oxide & Alternative Gate Dielectric Reliability**
  - **Burn In**
  - **NBTI**
- **Tutorials**
  - ***"Molecular Electronics: What will be the Reliability Issues?,"*** **J.S. Suehle, Semicond. Electronics Div., NIST**
  - ***"New Age Electromigration Testing,"*** **J.R. Lloyd, IBM TJ Watson Res. Ctr.**
- **30+ Technical Presentations on:**
  - **Thin Oxide Reliability**
  - **Copper Interconnects**
  - **Product Reliability**
  - **High-k Dielectrics**
  - **NBTI Phenomena**
  - **Hot Carrier Degradation**
- **Refereed/Open Poster Sessions**
- **Special Interest Groups**

Major Technical Themes

As industry retools and regroups for the coming technology sector expansion, it is crucial that the reliability of new materials, devices and products be kept at the forefront of development and design of new products. The Integrated Reliability Workshop is focused this year on exactly this mission.

The workshop begins with two tutorials on diverse, cutting-edge topics in materials and device reliability. They offer a unique opportunity for both newcomers and experienced researchers to gain insight into the next generation of techniques in reliability testing.

Molecular Electronics: What will be the Reliability Issues? will be presented by John Suehle from the Semiconductor Electronics Division at NIST. He brings many years of experience and international recognition in device and oxide reliability to the exciting new technology area of Molecular Electronics.

New Age Electromigration Testing will be presented by Jim Lloyd from IBM, a provocative speaker, innovative researcher, and international expert in metallization reliability. His tutorial will focus on the challenges associated with design and interpretation of reliability tests for Cu and Cu/Low-K systems.

This year the workshop features an invited talk, *Technology on the Edge*, by William Tonti, a long-time contributor to reliability innovation and IRPS 2002 General Chair. This stimulating presentation discusses technology changes needed to meet market driven product requirements.

Our keynote paper, *Embedded Non-Volatile Memory Qualification Methodologies for Automotive Applications*, picks up on the important theme of reliability of Non-Volatile Memories (NVM). Presenting this important paper is John Bridwell, Manager of Reliability & Device Analysis in the Embedded Memory Center at Motorola Semiconductor Products Sector. It promises to be a great beginning to our technical sessions and the stimulus for many conversations throughout the course of the workshop. Interested participants may even want to take this opportunity to set up a Special Interest Group on NVM!

As usual we will have ample time for one-on-one exchanges, organized discussion groups, our popular and productive SIGs (Special Interest Groups) and poster sessions where all our attendees are encourage to display a poster with their most recent work, ideas, and results. New this year will be the opportunity for our poster presenters to deliver a five-minute synopsis of their poster. This is a great opportunity for all workshop participants to gain a quick preview of what they can expect when they visit the full poster.

Tell your colleagues about the workshop! *You* and *they* need to attend.

Tell your manager! You and your organization cannot afford to miss this investment in learning to help you deal with today and to prepare for tomorrow.

–over–

KEYNOTE

Embedded Non-Volatile Memory Qualification Methodologies for Automotive Applications

John Bridwell, Manager, Reliability & Device Analysis
Embedded Memory Center, Technology & Manufacturing,
Motorola Semiconductor Products Sector

The reliability requirements from the automotive market place are demanding lower and lower lifetime failure rates. The market covers a wide range of applications from window controllers to safety critical applications such as air bag controllers. To meet customer demands of zero warranty failures, the successful introduction of embedded non-volatile memory requires a rigorous development methodology. This methodology must support the statistics necessary to meet the market expectations.

A development methodology has been defined that encompasses technology feasibility and certification in support of product qualifications. In following this method, the typical product qualification requirements can be met while enhancing the overall insight into the eNVM module's reliability. This methodology and the typical data that must be gathered and modeled during the development and product phases will be presented.

TUTORIALS

Chairs: Doug Menke,and Amr Haggag, Motorola

Tutorial #1 Monday 2:00 p.m. to 3:30 p.m.

Molecular Electronics: What will be the Reliability Issues?

John S. Suehle
Semiconductor Electronics Division, NIST

At some point in time the further miniaturization of microelectronics using current silicon-based technologies will become fundamentally difficult and prohibitively costly. Many experts predict that the exponential increase in transistor density and processing speed with time predicted by Moore's Law will saturate around or before 2015. Recently, there has been much excitement about the possibility of using single organic molecules as electronic switching devices. Several research groups have demonstrated single molecule switching devices and molecular MOSFETs. A molecular device is over 60,000 times smaller than a silicon transistor with a 120 nm channel length. A "molecular" Pentium processor would be able to fit in a 100 μm^2 area. This presentation will discuss the current state of research in molecular electronic devices including principals of operation and fabrication techniques. Challenges in device fabrication and characterization will be discussed. Finally, potential reliability failure mechanisms of single molecule devices will be hypothesized.

Tutorial #2 Monday 4:00 p.m. to 6:00 p.m.

"New Age Electromigration Testing"

Jim Lloyd
IBM T.J. Watson Research Center

The future ain't what it used to be. For the past 30 years electromigration testing in Al and Al/Cu alloys was relatively straightforward. We may have argued (incessantly) about the meaning of the results, but the methods and testing were pretty easy. This was primarily due to the forgiving nature of Al alloys and their relative insensitivity to the environment. Predicting the future was not always easy, but we grew to where we had some confidence that we could do so with reasonable accuracy.

With Cu we have new challenges. Cu is not so forgiving, the transport mechanism is different and the response to the testing environment is more important. Cu oxidizes in a completely different manner than Al. This makes huge differences in the electromigration performance, the way we extrapolate and treat data and the way we write design rules.

Cu and low-K dielectrics offer even more opportunity for creative reliability testing and interpretation. Low-k dielectrics are as strong as Jello, absorb like sponges and are virtually transparent to oxidation. Air bridges will be even more fun.

You can't predict the future the same way we did with Al. New learning is required. However, an understanding of the issues with the new materials will allow us perform tests meaningfully and make predictions just as reasonably.

In this 2 hour tutorial, the differences between Al alloys and Cu electromigration testing will be explained and the major issues pertaining to low-K dielectrics and electromigration testing, performance and design rule generation will be covered.

INVITED TALK

Tuesday 1:10 p.m. to 3:00 p.m.

Technology On the Edge

William R. Tonti
IBM MicroElectronics

The semiconductor industry is poised to enter a new era where extraordinary opportunities for new applications in pervasive markets will drive the push for higher circuit density, greater speeds, and better power dissipation. This push is at the heart of some of the latest advances that have occurred, including the integration of low-resistance conductors, insulated substrates, and band-gap engineered devices.

As an example, take the revolution in the cell phone industry moving from analog or 1G phones to the new 3G digital space integrating both voice and data. This market requires, at a minimum, devices that can achieve a data rate of 10GB/s migrating to 40GB/s. In short, the devices that switch at this rate did not exist two years ago, but today they are out of the research labs and in production.

The presentation is planned to be "interactive" in the sense of inviting direct audience involvement. It is expected that the commentary will be within the context of the list of topics that follows. But, those with other issues to share are invited to take part. In list form, these are the broad issues that are included for open interactive discussion:

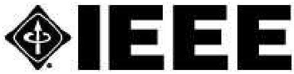
- Semiconductor Industry Trends
- Pervasive Computing
- Game Market
- Advanced materials
- CMOS / Bipolar Integration
- SOI
- Moore's Law contrasted with present scaling
- Nanotechnology
- Packaging
- Technology, and time to market

DISCUSSION GROUPS

Chairs: Prasad Chaparala, National Semiconductor Corp and Vijay Rajagopalan, LSI Logic

The evening discussion group program is regarded as a favorite highlight of the workshop experience. Attendees will have a choice of two areas on Tuesday and Wednesday evenings. The topics to be discussed will be at the discretion of those participating in the group. Each group is assigned a pair of leaders who have extensive

(continued on back of registration form)



2002 *International* INTEGRATED RELIABILITY WORKSHOP

PRELIMINARY PROGRAM

MONDAY, October 21

1:00 – 8:00 p.m.	Lodge check-in. Get room assignment (prearranged), room key, lodge area map, and information. (if physically challenged please notify desk of special needs)
1:00 – 6:00 p.m.	Registration: Pick up badges & handout. (*Dining Room Lounge*): Discussion Group Assignments, SIG Signup.
2:00 – 3:30 p.m.	**Tutorial #1:** "Molecular electronics: What will be the reliability issues?", *John S. Suehle, Semiconductor Electronics Division, NIST*
3:30 – 4:00 p.m.	Break
4:00 – 6:00 p.m.	**Tutorial #2:** "New age electromigration testing" *Jim Lloyd, IBM T.J. Watson Research Center*
6:15 – 7:30 p.m.	DINNER *(Dining Room)*: Introduction of workshop agenda, speakers dine with your Session Chair.
7:30 – 8:00 p.m.	Discussion Groups Assignments/SIG signup (*Dining Room Lounge*); Poster Preparation (*Old Lodge*)
8:00 – 9:00 p.m.	Short Oral Presentation Session I *(Cathedral Room)*
9:00 – 10:00 p.m.	Mixer & Poster Session *(Cathedral Room)*

TUESDAY, October 22

7:00 – 8:00 a.m.	BREAKFAST *(Dining Room)*
8:15 – 8:30 a.m.	Welcome & Introduction: Linda Head, General Chair & Gennadi Bersuker, Technical Program Chair *(Angora Room)*
8:30 – 9:30 a.m.	Keynote: "Embedded non-volatile memory qualification methodologies for automotive applications," *John Bridwell, Manager, Reliability & Device Analysis, Embedded Memory Center, Technology & Manufacturing, Motorola Semiconductor Products Sector*
9:30 – 9:50 a.m.	Break
9:50 – 11:40 a.m.	Session #1: Thin Oxide Reliability (TOR)
	TOR-1 "Evidence that the progressiveness is defect generation probability driven," F. Monsieur, E. Vincent, G. Ribes, S. Bruyere, D. Roy, STMicroelectronics, V. Huard, Philips Semiconductors, G. Pananakakis, G. Ghibaudo, IMEP/ENSERG
	TOR-2 "Defect generation in ultra-thin oxide over large fluence ranges," D. Heh, J. Bernstein, Univ. of Maryland, E.M. Vogel, NIST
	TOR-3 "Comparison of low leakage and high speed deep submicron PMOSFET's submitted to hole injection," A. Bravaix, D. Goguenheim, L2MP-ISEM, N. Revil, E. Vincent, STMicroelectronics
	TOR-4 "Conducting Atomic Force Microscopy studies for reliability evaluation of ultrathin SiO_2 films," G. Benstetter, W. Frammelsberger, University of Applied Sciences Deggendorf, T. Schweinboeck, R. Stamp, Infineon Technologies, J. Kiely, University of the West of England
	TOR-5 "Parametric reliability test: Wafer surface contamination study," G. Bersuker, J. Guan, G. Gale, P. Lysaght, D. Riley, H. Huff, International SEMATECH
11:40 – 12:00 p.m.	Group Picture
12:00 – 1:10 p.m.	LUNCH *(Dining Room)*
1:10 – 3:00 p.m.	Invited Talk: "Technology on the edge," Bill Tonti, IBM
3:00 – 3:30 p.m.	Break
3:30 – 4:50 p.m.	Session #2 Cu Interconnect I (CUI)
	CUI-1 "Adhesion and electromigration in Cu metallization," J. Lloyd, M. Lane, E. Liniger, IBM
	CUI-2 "Intra-metal leakage reliability characterization for the line/via combined structures in copper/low-k interconnect process," Jeung-Woo Kim, Nam-Hyung Lee, Hyung-woo Kim, Hyun-Soo Kim, Chae-Bog Rim, System LSI Div. Samsung Electronics Co.
	CUI-3 "Extrapolation of highly accelerated electromigration tests on copper to operation condition," J. von Hagen, R. Bauer, S. Penka, A. Pietsch, W. Walter, A. Zitzelsberger, Infineon Technologies AG
	CUI-4 "Temperature determination methods on copper material for highly accelerated electromigration tests (e.g. SWEAT)," J. von Hagen, Infineon Technologies AG, H. Schafft, NIST
4:50 – 5:00 p.m.	Break
5:00 – 6:00 p.m.	Session #3 Cu Interconnect II (CUI)
	CUI-5 "A practical methodology for multi-modality electromigration lifetime prediction," M. H. Lin, G. S. Yang, Y. L. Lin, C. Y. Wu, C. C. Lin, M. S. Yeh, E. Hsiung, K. P. Chang, K. C. Su, J. K. Chen, Y. J. Chang, United Microelectronics Corp.
	CUI-6 "Electromigration simulation of Cu Low-k multi-level interconnect segment," V. Sukharev, R. Choudhury, C. W. Park, LSI Logic Corp.
	CUI-7 "Effect of reduced current density stress on the results of isothemal electromigration test for Cu damascene lines," Kin Leong Yap Andrew, Bee Hoon Lim, Chartered Semiconductor Manufacturing
6:00 – 7:30 p.m.	DINNER *(Dining Room)*
7:30 – 9:00 p.m.	Discussion Groups: Chair: Prasad Chaparala, NSC (90 min. parallel sessions for each topic) Attendees are to participate in one of the groups: 1) Electromigration, 2) Ultra Thin Oxide & Alternative Gate Dielectric Reliability, 3) Burn In, 4) NBTI
9:00 – 10:30 p.m.	Individual SIG Meetings (To be announced at the Camp.)

WEDNESDAY, October 23

7:00 – 8:00 a.m.	BREAKFAST *(Dining Room)*
8:00 – 8:15 a.m.	Announcements *(Angora Room)*
8:15 – 9:15 a.m.	Session #4 Product Reliability (PRR)
	PRR-1 "Gate reliability correlation between test structure and DRAM product chips," R. Vollertsen, K. Nierle, IBM/Infineon, E. Wu, IBM
	PRR-2 "Time-dependent dielectric breakdown evaluation of deep trench capacitor With sidewall hemispherical-grained silicon for Gigabit DRAM technology," F. Chen, A. Strong, P. Parkinson, K. Settlemyer, R. Jammy, J. Li, IBM, M. Ruprecht, H. Tews, M. Seitz, M. Kim, I. McStay, R. Reviere, Infineon Technologies,
	PRR-3 "Fast wafer level monitoring of stress induced leakage current in deep sub-micron embedded non-volatile memory processes," G. Tao, A. Scarpa, H. Valk, L. van Marwijk, K. van Dijk, F. Kuper, Phillips Semiconductors
9:15– 9:25 a.m.	Break
9:25 – 10:25 a.m.	Session #5: Product Reliability II (PRR)
	PRR-4 "Wafer-level assessment of SiGe NPN HBTs after high temperature electrical operation," K. Hofmann, G. Bruegmann, A. Lili, Infineon Technologies AG

	PRR-5	"Fast and reliable WLR monitoring methodology for assessing thick dielectrics test structures integrated in the kerf of product wafers," A. Martin, J. von Hagen, J. Fazekas, K. Allers, Infineon Technologies AG
	PRR-6	"Direct correlation of electrical reliability data to SEM analysis for deep trench dielectric weakness," M. Wuhn, G. Diestel, M. Obry, Infineon Technologies AG
10:25– 10:40 a.m.	Break	
10:40 – 12:00 p.m.	Session #6 High-K Dielectrics (HKD)	
	HKD-1	"Polarity dependent reliability of advanced MOSFET using MOCVD nitrided Hf-silicate high-k gate dielectric," J. Zhang, E. Shao, Q. Xiang, J. Chan, J. Jeon, J. Goo, A. Marathe, B. Ogle, M. Lin, K. Taylor, AMD
	HKD-2	"Thermal and dielectric breakdown for metal insulator metal capacitors w/ tantalum pentoxide dielectric," K. Allers, R. Schwab, W. Walter, M. Schrenk, H. Korner, Infineon Technologies AG
	HKD-3	"Reliability concerns for HfO_2/Si devices: Interface and dielectric traps ," A. Kang, P. Lenahan, Penn State University, J. Conley, Sharp Labs of America
	HKD-4	"Electrical propeties and reliability of HfO_2 deposited via ALD," J. Conley, Y. Ono, W. Zhuang, L. Stecker, Sharp Labs of America
12:00 – 1:30 p.m.	LUNCH *(Dining Room)*: Take out Lunch bags available.	
1:30 – 5:00 p.m.	Open	The afternoon is free for discussion, hiking & other recreation; or for viewing videos. Titles of Videos will be available at the Workshop
5:00 – 5:30 p.m.	Short Oral Presentations Session II *(Cathedral Room)*	
5:30 – 6:00 p.m.	Mixer & Poster Session *(Cathedral Room)*	
6:00 – 7:30 p.m.	DINNER *(Dining Room)*	
7:30 – 9:00 p.m.	Discussion Groups: Chair: Prasad Chaparala, NSC (90 min. parallel sessions for each topic) Attendees are to participate in one of the groups: 1) Electromigration, 2) Ultra Thin Oxide & Alternative Gate Dielectric Reliability, 3) Burn In, 4) NBTI	
9:00 – 10:30 p.m.	Individual SIG Meetings	

THURSDAY, October 24

7:00 – 8:00 a.m.	BREAKFAST (*Dining Room*)	
8:15 – 8:30 a.m.	Announcements *(Angora Room)*	
8:30 – 9:50 a.m.	Session #7 Hot Carrier Degradation (HCD)	
	HCD-1	"Bias and temperature dependent hot-carrier characteristics of sub-100 nm partially depleted SOI MOSFET's," E. Zhao, J. Chan, J. Zhang, A. Marathe, K. Taylor, AMD
	HCD-2	"Hot-carrier degradation of n-channel MOS LDD devices under dynamic stress conditions," E. King, R. Lacoe, The Aerospace Corporation
	HCD-3	"Hot carrier luminescence for backside 0.15 µm CMOS device analysis," W. Ng, G. Gao, National Semiconductor, A. Abraham, T. Lundquist, Schlumberger Probe Systems
	HCD-4	"1-D and 2-D hot carrier layout optimization of N-LDMOS transistor arrays," D. Brisbin, A. Strachan, P. Chaparala, National Semiconductor Corp.
9:50 – 10:10 a.m.	Break	
10:10 – 11:30 a.m.	Session #8 NBTI Phenomena (NBT)	
	NBT-1	"Negative bias temperature instability of deel sub-micron p-MOSFETs under pulsed bias stress," B. Zhu, J. Bernstein, University of Maryland, J. Suehle, NIST, Y. Chen, Agere Systems
	NBT-2	"The impact of NBTI and HCI on deep sub-micron PMOSFETs' lifetime," Chul-Hee Jeon, Sam-Young Kim, Hyun-Soo Kim, Chae-Bog Rim, Samsung Electronics
	NBT-3	"Model for NBTI in p-MOSFETs with ultra thin nitrided gate oxides," M Houssa, J. Autran, L2MP, C.Parthasarathy, N. Revil, E. Vincent, STMicroelectronics, V. Huard, Philips Semiconductors
	NBT-4	"Interface traps and oxide charges during NBTI stress in p-MOSFET," V. Huard, Philips Semiconductors, F. Monsieur, C. Parthasarathy, S. Bruyere, STMicroelectronics
11:30 – 12:00 p.m.	Wrap-Up	
12:00 – 1:30 p.m.	LUNCH *(Dining Room)*— & then the Workshop Ends—Leave the Stanford Sierra Camp unless attending JC14.2	
2:00 p.m.	JEDEC 14.2 Committee on Wafer Level Reliability Meeting	

2002 IRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 24-25)

(Please type, print or attach business card)

Meeting registration automatically includes a room reservation.

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ADVANCE REGISTRATION FEES

IEEE Member ______________ **$945*** __________
(member No. Req'd)

NON-IEEE Member .... **$995*** __________

** Includes workshop attendance & handout materials, tutorial attendance, 3 nights lodging (Monday—Wednesday) 9 meals (dinner Monday—lunch Thursday), Final Workshop Report.*

EXTRA COPIES of Workshop Final Report ....Qty: ______ x **$80** __________

JC-14.2 Mtg. accommodations** **$180** __________

*** Includes 1 night lodging (Thursday), 3 meals (dinner Thursday— lunch Friday)*

TOTAL REMITTED $ __________

Cancellation fees: $50 after Sept. 27 ; full fee after Oct. 11

Send this completed form and payment to:
IRW Registration; P.O. Box 308; Westmoreland, NY 13490

Paying by credit card... fax to 315-336-9134
Questions? becky@sar101.com or 315-339-3968
or web site: http://www.irps.org/irw
Wire Transfer (add $30 for bank fees) call for details

TAHOE CASINO EXPRESS: The Tahoe Casino Express **runs from Reno to Tahoe** between 6 a.m. and midnight with departures from Reno at: 6:15 a.m., 8:15 a.m., 9:15, 10:15, 11:15, 12:15 p.m., 1:15, 2:15, 3:15, 5:30, 7:30, 9:30, and 12:30 a.m. The Express costs $19 each way ($34 round trip) and tickets can be purchased at the Express counter located in the baggage area in the Reno airport. Travel time is approximately 1½ hours. The Casino Express can be reached at 800-446-6128. The Express **leaves the Horizon Casino at Lake Tahoe and returns to Reno** on the following schedule: 4:10 a.m., 6:10, 8:10, 9:10, 10:10, 11:10, 12:10 p.m., 1:10, 2:10, 3:10, 4:10, 5:10, 7:25, and 10:25 p.m. Tickets may be purchased in the Horizon Casino at the main cashier's cage. For more information check http://www.tahoecasinoexpress.com.

Stanford Sierra Camp offers courtesy transportation for conference attendees from the Horizon Casino between 10 a.m. and 10 p.m. on Registration Day (Monday, Oct. 21). Return trips to the Casino are offered on the last day of the conference only. If you are planning on using the Casino Express, please notify Stanford Sierra Camp (530-541-1244) at least ONE WEEK prior to your arrival date. If you find yourself stranded, please call the camp at the same number. The IRW Arrangements Committee may be able to provide emergency service to and from the casino.

DISCUSSION GROUPS *(continued from page 2)*

experience with the area and will help to guide the discussion. Everyone is encouraged to bring along data and/or ideas to share on topics that are of particular interest. As we get closer to the date of the workshop, we will be surveying registered attendees so that we may prepare relevant discussion outlines to be distributed at the camp. This year's discussion areas and leaders are:

Electromigration

Jim Lloyd, IBM and Harry Schafft, NIST

Discussion will cover electromigration issues in both Al and Cu metallization systems. Focal points for discussion will be on wafer level vs package level EM, high temperature testing, failure criteria, data analysis and interpretation.

Ultra thin Oxide and Alternative Gate Dielectric Reliability

John Conley Jr., Sharp Labs Of America

Intense research work is underway in the industry to find a gate dielectric material that can replace silicon dioxide. Discussion will be on status of the leading candidate materials and reliability requirements for these next-generation gate dielectrics.

Burn In

Bill Tonti, IBM

Discussion will be on evaluating recent developments in Burn In area and possible strategy changes to address future needs. Areas of discussion will also include wafer-level Burn In, efficient screening methodologies and on ways to reduce Burn In costs.

NBTI

Negative Bias Temperature Instability (NBTI) has becoming a major reliability concern in advanced CMOS technologies. A full session on NBTI at this year's workshop reflects the growing interest in this area. Discussion will be on current understanding of the mechanism, test methodologies and failure criteria.

SPECIAL INTEREST GROUPS

Chair: Prasad Chaparala, National Semiconductor Corp and Vijay Rajagopalan, LSI Logic

The Special Interest Groups (SIGs) program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal in our SIGs. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. Anyone interested in more information on SIGs see http://www.irps.org/irw/sig/.

REFEREED & OPEN POSTER SESSIONS

(Monday & Wednesday Evening)

Chairs: Emmanuel Vincent, ST Microelectroonics and Nguyen Bui, Lattice Semiconductor

All attendees have the opportunity to present a poster to communicate and discuss their ideas and newest results on technical projects or issues. This year we are instituting a new opportunity for our poster presenters. There will be time set aside at the beginning of each poster session for you to present a 5 minute synopsis of your poster - please bring overhead transpariences (4 or 5 at most!) if you wish to present at this session. Please indicate on the registration form your intention to bring a poster by reserving a poster display board (32" × 40" or 81 cm × 100 cm) in the space provided. Your work should be in Landscape format on 8½ × 11" or A4 paper with a maximum of twelve pages. In addition, you are invited to submit a two-page abstract of your poster presentation for inclusion in the Workshop Final Report. See www.irps.org/irw/poster/ for details and deadlines. This is a great opportunity for you to share your work with your peers. If you are presenting a refereed or invited poster a display board will be reserved for you.

JEDEC 14.2 MEETING. The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is $180.00, which includes Thursday night dinner and lodging *and* Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558 or www.jedec.org, or call Mike Dion, JC-14.2 Chair at (407) 724-7067.

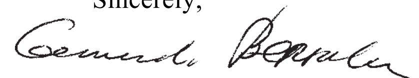
MORE INFORMATION. We expect an exciting workshop again this year. We look forward to your active participation in the many Workshop activities and your valuable contribution to the technical discussions. If you have additional questions, please contact either: the Technical Program Chair, Gennadi Bersuker, by phone 512-356-7045, email: gennadi.bersuker@sematech.org; the Tech. Prog. Vice Chair, Alvin Strong, By phone: 802-769-1326, email: astrong@us.ibm.com; or the General Chair, Linda Head, by phone, 856 256 5335, fax…5241, or email: head@rowan.edu; Web site: www.irps.org/irw.

REGISTER NOW!

Complete and send in the enclosed registration form. Please register early. We have sold out in past years. Space at the Camp limits IRW to roughly 120 attendees.

We look forward to seeing you at the Workshop!

Sincerely,



Gennadi Bersuker
Technical Program Chair

RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees.

ACCOMMODATIONS

The Stanford Sierra Camp provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note; while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. Towels and soap are provided. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

- **All participants must stay at the camp during the workshop.**
- **We cannot accommodate spouses or any companions at the camp**.
- **Accommodations are *not* available at the Stanford Camp for any day before or after the workshop.**
- Smoking is permitted outdoors only. Smoking is not be permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3968.
- A message board will be available for incoming calls, (530) 541-1244. There are pay telephones for outgoing calls. There are no telephones in the rooms.

ARRANGEMENTS INFORMATION

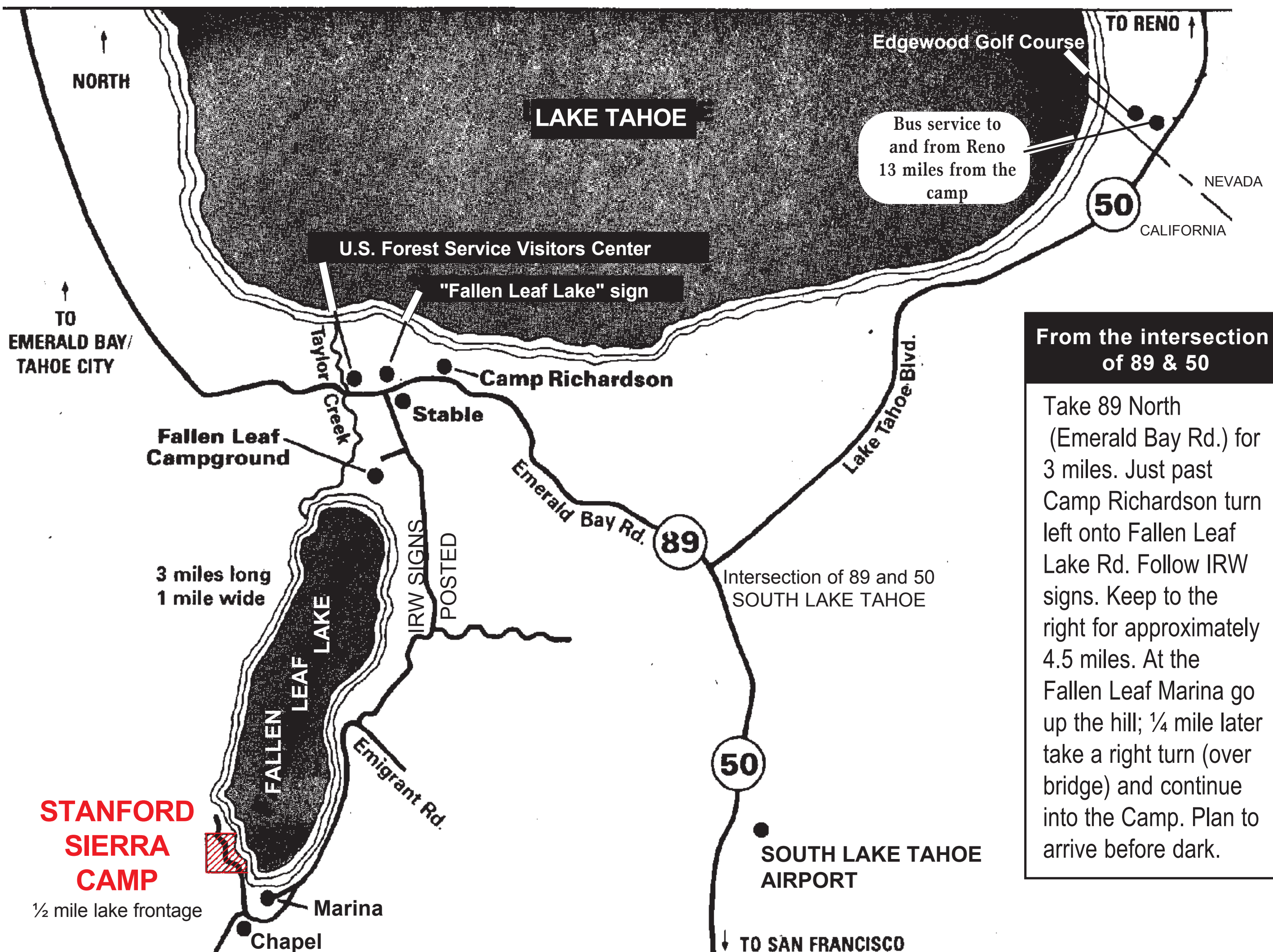
Special discounted airfares for IRW have been negotiated by IEEE Global Travel Services. Please note that this service can be used by attendees traveling from within or outside of the United States and Canada. Discounts are as high as 20% off the lowest published airfares with American, TWA, Continental and United airlines. Special rates have also been negotiated with Avis Rental Car Company. Travel arrangements using the negotiated air carriers or the carriers of your choice can be made through IEEE Global Travel Services by calling between the hours of 8:30 a.m. and 5:30 p.m. EST. Monday through Friday. Within the US and Canada, call 800-879-4333; and outside of the US and Canada, call +1 732-562-5387. Or, visit their on-line travel service web site at www.ieeetravelonline.org. At this secure site you can search, reserve, and ticket your travel anytime, anywhere. You may also fax your requirements to the IEEE Global Travel Services at 732-562-8815. When faxing, please be sure to include your travel dates, departure, return times, phone and fax numbers and mention the IEEE IRW. A Travel Counselor will contact you promptly.

TRANSPORTATION NOTE: The Stanford Sierra Camp is located on Fallen Leaf Lake, a few miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Reno is approximately two hours from the Stanford Sierra Camp. Currently no commercial flights are available to the South Lake Tahoe Airport.

- Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the ***Tahoe Casino Expres***s. For ***Tahoe Casino Express*** schedule details see back of this page, call 800-446-6128, or check http://www.tahoecasinoexpress.com.

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the camp. A small flashlight would be helpful to find your cabin after dark.



From the intersection of 89 & 50

Take 89 North (Emerald Bay Rd.) for 3 miles. Just past Camp Richardson turn left onto Fallen Leaf Lake Rd. Follow IRW signs. Keep to the right for approximately 4.5 miles. At the Fallen Leaf Marina go up the hill; ¼ mile later take a right turn (over bridge) and continue into the Camp. Plan to arrive before dark.