

# 2004 IEEE INTERNATIONAL INTEGRATED RELIABILITY WORKSHOP PROGRAM



**MONDAY, October 18** Please have lunch before arriving at the camp; no lunch will be served at the camp.  
 1:00 – 6:00 p.m. Registration: Pick up badges & handout (*Dining Room Lounge*) Discussion Group and SIG Signup; Poster preparation  
 1:00 – 8:00 p.m. Lodge check-in. Get room assignment (prearranged) & room key, with lodge area map and information.  
 (if physically challenged please notify desk of special needs)  
 1:30 – 3:30 p.m. **Tutorials A & B** (parallel sessions) • A: High-K dielectric Tutorials • B: Oxide & Product Reliability Tutorials  
 3:30 – 4:00 p.m. Break (poster preparation)  
 4:00 – 6:00 p.m. **Tutorials C & D** (parallel sessions) • C: Interconnects Tutorials • D: NBTI Tutorials  
 6:15 – 7:20 p.m. DINNER, (*Dining Room*) authors: dine with your session chair  
 7:20 – 7:30 p.m. Announcements, DGs, SIGs (*Cathedral Room*)  
 7:30 – 8:45 p.m. Mixer & Poster Session 1 (*Cathedral Room*)  
 8:45 – 9:30 p.m. Mini Workshop “Mentoring in the Technical Environment” by Deborah Massey, IBM (15min presentation before panel discussion) (*Angora Room*)

**TUESDAY, October 19**  
 7:00 – 8:00 a.m. BREAKFAST (*Dining Room*)  
 8:15 – 8:30 a.m. Welcome & Introduction: Alvin Strong, General Chair & Technical Program Overview: Rolf Vollertsen, Tech. Prog. Chair (*Angora Room*)  
 8:30 – 9:30 a.m. Keynote: “Managing Tomorrow’s Reliability Risks Today” by Timothy Forhan, AMI Semiconductor  
 9:30 – 9:50 a.m. Break  
 9:50 – 11:30 a.m. Session #1A (*Angora Room*) and 1B (*Cathedral Room*) parallel

## Session #1A: Gate Oxide - SiO<sub>2</sub> (GO1)

Chairs: Bin Wang, Impinj & Rolf Vollertsen, Infineon

- GO1-1 Modeling Charge to Breakdown using hydrogen multi-vibrational excitation (Thin SiO<sub>2</sub> and high-K dielectrics)—Guillaume Ribes, S. Bruyère, M. Denais, F. Monsieur, V. Huard, D. Roy, G. Ghibaud, STM
- GO1-2 Hydrogen release and defect generation rate in ultra-thin oxides—Vincent Huard, Philips and M. Denais, F. Monsieur, STM
- GO1-3 Gate Oxide Reliability and Deuterated CMOS Processing—A.J. Hof, A.Y. Kovalgin, J. Schmitz, MESA, R. van Schaijk, W.M. Baks, Philips
- GO1-4 A Novel Explanation of Power-Law Model with Quantitative Hydrogen Mechanism for Ultra-thin Oxide PMOS—Jerry Shieh, Sinclair Chiang, Kevin Kang, K.C. Su, UMC

11:30 – 12:00 p.m. Group Picture  
 12:00 – 1:00 p.m. LUNCH, *Dining Room*  
 1:00 – 2:40 p.m. Session #2A (*Angora Room*) and 2B (*Cathedral Room*) parallel

## Session #2A: Gate Oxide - SiO<sub>2</sub> (GO2)

Chairs: Joachim Reiner, EMPA & Sylvie Bruyère STM

- GO2-1 A Temperature Accelerated Model for High State Retention Loss of Nitride Storage Flash Memory—Ming-Yi Lee, N. K. Zous, Trista Huang, W. J. Tsai, Albert Kuo, Tahui Wang, Shaw Yin, Chih-Yuan Lu, Macronix International
- GO2-2 Reliability Response of Plasma-Nitrided Gate Dielectrics to Physical and Electrical CET-Scaling—R. Geilenkeuser, K. Wiczorek, T. Mantei, F. Grätsch, L. Herrmann, J.-O. Weidner, AMD
- GO2-3 New Gate Oxide wear-out model for accurate Device Lifetime predictions on vertical Drain NMOSFET—Sangwoo Pae, et al. Intel
- GO2-4 Impact of Buried Layer Processing on Gate Oxide Integrity—Barry O’Connell, Robert Yang, Wipawan Yindeepol, Joseph De Santis, Andy Strachan, William Coppock, Richard Foote, Charles Dark, Prochy Sethna, Prasad Chaparala, NSC

2:40 – 3:00 p.m. Break  
 3:00 – 4:40 p.m. Session #3A (*Angora Room*) and 3 B (*Cathedral Room*) parallel

## Session #3A: Gate Oxide - SiO<sub>2</sub> (GO3)

Chairs: Bill Knowlton, Boise State & Yuan Chen, JPL

- GO3-1 Study of Stress-induced Leakage Current and its effect on Charge Loss of 70A Logic Nonvolatile Memory Cell Using Floating-Gate Integrator Technique—Bin Wang, Chih-Hsin Wang, Yanjun Ma, Todd Humes, Chris Diorio, Impinj
- GO3-2 Survey of Soft Breakdown (SBD) in 2.0 nm Gate Oxides in MOS Devices and Inverter Circuits—Mike L. Ogas, G. Southwick III, B. J. Cheek, R. J. Baker, G. Bersuker, W. B. Knowlton, Boise State
- GO3-3 Reversible leakage current switching in thin gate oxides – soft breakdown or noise?—Joachim Reiner, EMPA
- GO3-4 Fast Wafer Level Data Acquisition for Reliability Characterization of sub-100 nm CMOS Technologies—Andreas Kerber, Martin Kerber, Infineon Techn.

4:40 – 6:00 p.m. Poster Session 2 (*Cathedral Room*)  
 6:00 – 7:30 p.m. DINNER, *Dining Room*  
 7:30 – 9:00 p.m. Discussion Groups: Chair: Sylvie Bruyère STMicroelectronics  
 (90 minute parallel sessions for each topic) Attendees are to participate in one of the groups  
 9:00 – 10:30 p.m. Individual SIG Meetings (to be announced at camp)

## Session #1B: Interconnects (IC1)

Chairs: Harry Schafft, NIST & Lynett Westergard, AMI Semi.

- IC1-1 Thermal and Electromigration Challenges for Advanced Interconnects—Baozhen Li, Dave Harmon, Jason Gill, Fen Chen, Timothy Sullivan, IBM
- IC1-2 Analytical extraction of thermal conductivity of low k dielectrics and application in RMS current determination in interconnects for advanced technologies—David Ney, V. Girault, STM, X.Federspiel, Philips
- IC1-3 Modeling Interconnect Behavior with a Calibrated FEA Model—Alvin Strong, Fen Chen, IBM

## Session #2 B: Interconnects (IC2)

Chairs: Tim Sullivan, IBM & Dave Catlett, TI

- IC2-1 90nm node Damascene Copper Stress Voiding Model and lifetime extrapolation Methodology—Xavier Federspiel, S. Orain, Philips
- IC2-2 Electromigration in Damascene Copper Lines, an essential Design Choice for Life time prediction—Valerie Girault, F. Terrier, STM
- IC2-3 Modeling global thinning of copper metallization for integrated circuits under electromigration stress—Jun-Ho Choy, Yan Zhang, Karen L. Kavanagh, Simon Fraser Univ.
- IC2-4 A model for electromigration-induced degradation mechanisms in dual-inlaid copper interconnect structures: Effect of interface bonding strength—Valeriy Sukharev, LSI Logic, Ehrenfried Zschech, AMD

## Session #3 B: Interconnects (IC3)

Chairs: Deb Massey, IBM & Harry Schafft, NIST

- IC3-1 Electromigration-limited lifetime of aluminum bond pads—Martina Hommel, Sabine Penka, Franz Ungar, Infineon Technologies
- IC3-2 Electromigration of MRAM-customized Cu Interconnects with Cladding Barriers and Top Cap—Donald Gajewski, et al., Freescale Semiconductor

### WEDNESDAY, October 20

- 7:00 – 8:00 a.m. BREAKFAST (*Dining Room*)  
8:00 – 8:15 a.m. Announcements, (*Angora Room*)  
8:15 – 9:30 a.m. **Session #4 Hot Carriers (HCS)** — Chairs: Bill Tonti, IBM & Guoqiao Tao, Philips
- HCS-1 A Comprehensive Analysis of NFET Degradation due to Off-State Stress—Karl Hofmann, S. Holzhauser, C.Y. Kuo, Infineon Techn.  
HCS-2 New Insights into Threshold Voltage Shifts for Ultrathin Gate Oxides—Dawei Heh, Eric M. Vogel, and Joseph B. Bernstein, NIST  
HCS-3 Anomalous NMOSFET Hot Carrier Degradation Due to Hole Injection in a DGO CMOS Process—Doug Brisbin, Yuri Mirgorodski, Prasad Chaparala, NSC
- 9:30 – 9:50 a.m. Break  
9:50 – 11:30 a.m. **Session #5 NBTI (NBT)** — Chairs: Amr Haggag, Freescale & Greg Massey, IBM
- NBT-1 Oxide field dependence of interface trap generation, during Negative Bias Temperature Instability in PMOS—Mickael Denais, V. Huard, C. Parthasarathy, G. Ribes, F. Perrier, N. Revil, A. Bravaix, STM and Philips  
NBT-2 Mechanism of Dynamic NBTI in Deep Sub-Micron p-MOSFETs—Baozhong Zhu, S. Suehle, J. B. Bernstein, Y. Chen, NIST  
NBT-3 Atomic Scale Defects Involved in NBTI—J.P. Campbell, P.M. Lenahan, Penn State Univ., A.T. Krishnan, S. Krishnan, TI  
NBT-4 New hole trapping characterization during NBTI in 65nm node technology with distinct nitridation processing—Mickael Denais, A. Bravaix, V. Huard, C. Parthasarathy, M. Bidaud, G. Ribes, D. Barge, L. Vishnubhotla, B. Tavel, Y. Rey-Tauriac, F. Perrier, N. Revil, F. Arnaud, P. Stolk, STM and Philips
- 12:00 – 1:30 p.m. LUNCH (*Dining Room* — Take out Lunch bags available)  
1:30 – 5:00 p.m. Open The afternoon is free for discussion, IEEE video viewing (on demand), hiking & other recreation;  
5:00 – 6:15 p.m. Poster Session 3 (*Cathedral Room*)  
6:15 – 7:30 p.m. DINNER, (*Dining Room*)  
7:30 – 9:00 p.m. Discussion Groups, Chair: Sylvie Bruyère STMicroelectronics  
(90 minute parallel sessions for each topic) Attendees are to participate in one of the groups  
9:00 – 10:30 p.m. Individual SIG Meetings

### THURSDAY, October 21

- 7:00 – 8:00 a.m. BREAKFAST (*Dining Room*)  
8:15 – 8:30 a.m. Announcements, (*Angora Room*)  
8:30 – 10:35 a.m. **Session #6 High-k (HIK)** — Chairs: Chad Young, Sematech & John Conley, Sharp Labs
- HIK-1 Trapping and detrapping mechanism in hafnium based dielectrics characterized by pulse gate voltage techniques—Guillaume Ribes, S. Bruyère, D. Roy, M. Denais, V. Huard, M. Müller, T. Skotnicki, G. Ghibaudo, STM and Philips  
HIK-2 Effects of drain to gate stress on NMOSFET with polysilicon/Hf-silicate gate stack—Rino Choi, B. H. Lee, C. D. Young, J. H. Sim, K. Mathews, G. Bersuker, P. Zeitzoff, Sematech  
HIK-3 Recovery of NBTI degradation in HfSiON/Metal Gate Transistors—Rusty Harris, Rino Choi, B. H. Lee, C. D. Young, J. H. Sim, K. Mathews, P. Zeitzoff, P. Majhi, and G. Bersuker, Sematech  
HIK-4 Hot carrier stress study in Hf-silicate NMOS transistors—Johnny Sim, B. H. Lee, R. Choi, S. C. Song, C. D. Young, P. Zeitzoff, G. Bersuker, Sematech  
HIK-5 Mobility Evaluation in High-K Devices—Gennadi Bersuker, P. Zeitzoff, J. Sim, B. H. Lee, R. Choi, G. Brown, C. Young, SEMATECH
- 10:35 – 11:00 a.m. Break  
11:00 – 11:20 a.m. Discussion Group Summaries  
11:20 – 11:40 a.m. SIG Report  
11:40 – 12:00 p.m. Wrap-Up  
Noon – 1:20 p.m. LUNCH, (*Dining Room*) & then the Workshop Ends—Leave the Stanford Sierra Camp unless attending JC14.2  
2:00 p.m. JEDEC 14.2 Committee on Wafer Level Reliability Meeting