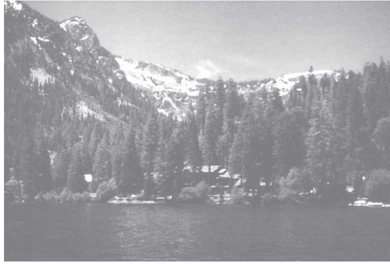
2005 *IEEE International*

INTEGRATED RELIABILITY WORKSHOP



October 17-20, 2005 **Stanford Sierra Conference Center, Lake Tahoe, CA** **http://www.iirw.org**

SECOND CALL FOR PAPERS

The Integrated Reliability Workshop focuses on ensuring semiconductor reliability through fabrication, design, testing, characterization, and simulation, as well as identification of the defects and physical mechanisms responsible for reliability problems. Through tutorials, discussion groups, and the informal format of the technical program, a unique environment is provided for understanding, developing, and sharing reliability technology for present and future semiconductor applications as well as ample opportunity for discussions and interactions with colleagues.

This year we especially welcome interconnect, product, novel device, and new technology submissions. Hot reliability topics for the workshop include: high-κ and nitrided SiO_2 gate dielectrics, product reliability and burn-in, NBTI, Cu interconnects and low-κ dielectrics, reliability modeling and simulation, SiGe and strained Si, III-V, SOI, optoelectronics, single event upsets, and reliability assessment of novel devices and future "nano"-technologies.

We invite you to submit a presentation proposal that addresses any integrated semiconductor related reliability issue, including the following topics:

- **DESIGNING-IN RELIABILITY (PRODUCTS, CIRCUITS, PROCESSES):**
  methodologies and concepts, modeling and simulation tools, reliability-driven design rules and checkers, use of WLR for design rule verification, process damage, demonstrated links between process, yield, and reliability.
- **CUSTOMER PRODUCT RELIABILITY REQUIREMENTS / MANUFACTURER RELIABILITY TASKS:**
  limits to achieving future reliability targets, reliability evaluation methodologies and reporting systems, data bases, wafer and package burn-in, packaging, strategies to eliminate burn-in.
- **ROOT CAUSE DEFECTS, PHYSICAL MECHANISMS, & SIMULATIONS**
  nature of defects, physical and electrical characterization of defects, defect generation models, modeling/simulation of reliability related circuit constraints, accelerated testing and lifetime extrapolation..
- **IDENTIFICATION AND CHARACTERIZATION OF NEW RELIABILITY EFFECTS:**
  failure mechanisms in new materials and device structures, reliability aspects of: high-k gate stack, Cu interconnects and low-k dielectrics, MOS and bipolar transistors including FinFETs and 3D gates, SiGe and strained Si, SOI, MEMS devices, new memory technologies, MRAM, nanotechnology reliability assessment, and limits to accelerated stressing.
- **DEEP SUB-MICRON TRANSISTOR AND CIRCUIT RELIABILITY:**
  single event effects and soft errors, ESD, electromigration, mechanical stress related issues, hot carrier effects, NBTI, dielectric breakdown, reliability extrapolation, impact of new material systems, modeling and simulation, impact of scaling,
- **WAFER LEVEL RELIABILITY TESTS, TEST APPROACHES, AND RELIABILITY TEST STRUCTURES:**
  fast stress tests and analysis methodologies, reduction in development time, in-line monitors, relation to circuit-element and package-level tests, use and interpretation of WLR data, success stories, fine tuning of WLR implementation, accounting for censoring, design, characterization, and data analysis for chip or package level circuit-like structures (including electrical and/or physical test/analysis).

SUBMISSION DEADLINE: *July 1, 2005*

Your *two page extended abstract* (maximum two pages including figures) should state clearly and concisely the results of your work and why they are significant. Representative data and/or figures that support your proposal are REQUIRED.

Please e-mail your abstract to the Technical Program Chair *either as an MS Word document or .pdf attachment,* further submission details can be found on the IIRW website. Fax submissions of abstracts will NOT be accepted. A separate covering letter must include your full business address, i.e., author name, affiliation, address, telephone and fax numbers, and the e-mail address for each co-author. State whether *oral or poster* presentation is preferred. All submissions will be acknowledged by email within three weeks. If you do not receive acknowledgment of your submission, please contact the Technical Program Chair.

Viewgraphs for all accepted oral presentations are required by September 7, 2005 for inclusion in the Presentation Handout that is distributed at the workshop. A written version of your presentation is due at the workshop for inclusion in the well known Final Report.

Technical Program Chair: John F. Conley, Jr.
Sharp Labs of America
5700 NW Pacific Rim Blvd.
Camas, WA 98607
360/834-8668
jconley@sharplabs.com

LODGING & FACILITIES

Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, a few miles from South Lake Tahoe, are clusters of 2 and 3 bedroom cabins furnished in the rustic style of an alpine resort. Each cabin is equipped with shared bathroom facilities. All rooms have decks with magnificent views of Fallen Leaf Lake and/or the surrounding Sierra peaks.

The physical isolation of the location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees.

Lodging can only be provided to registered attendees of IRW in accordance with housing rules.

HISTORY

The Wafer Level Reliability Workshop was initiated in 1982 through the efforts of O. D. "Bud" Trapp, of Technology Associates, and the active support and encouragement of DARPA (Defense Advanced Research Projects Agency). This support continued for the first eight years of the Workshop and included active support and involvement of the Stanford University Integrated Circuits Laboratory and the University of California, Berkeley, Dept. of Electrical Engineering and Computer Sciences. After DARPA sponsorship ended, Bud Trapp continued the direction of the Workshop until 1991 after which time he requested that sponsorship and management be assumed by an appropriate professional association. The IEEE accepted this responsibility in 1992. In 1993, the name of the Workshop was changed to the Integrated Reliability Workshop. This change reflects the enlarged scope of the Workshop, the integrated nature of reliability in the manufacture of semiconductor products, and the need for a broader and a more comprehensive approach to reliability engineering.

SPONSORS

The International Integrated Reliability Workshop is sponsored and managed by the IEEE Electron Device Society and the IEEE Reliability Society through the Board of Directors of the International Reliability Physics Symposium (IRPS).

MORE INFORMATION

For more details and updates on tutorial topics and speakers, discussion group topics, special interest groups, and the keynote address, including registration information, pictures of the area around camp, as well as topics presented at the workshop in previous years, please see our web-page:

http://www.iirw.org