

A Novel In-Process Wafer-Level Screening Technique for CMOS Devices

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Assurance of gate oxide integrity has been one of the most important issues for MOS devices, and extensive efforts have been made to decrease gate oxide defects from viewpoints of fabrication process improvement and defect screening. However, no process has been established to ensure perfect gate oxides quality while conventional screening such as burn-in is usually performed on finished products so that it is impossible to activate all nodes for screening by external signals through I/O circuits during burn-in. In this study, we have developed a novel in-process wafer-level screening technique for CMOS device which resolves the above difficulties. This technique can be easily implemented to any CMOS technologies. We show the details of the technique and experimental data supporting the idea behind this technique. Finally we demonstrate the effectiveness of this technique integrated into the 0.8 μ m double-metal CMOS technology.

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Ichiro Yoshii received his B.S. from Kyoto University (1980) and M.S. from Nagoya University (1982) both in physics, and Ph.D. in electrical engineering from Nagoya University (1995). He joined Toshiba Corp. in 1985 and has been involved in the process integration and reliability of CMOS. Currently he is a manager of quality and reliability for CMOS logic products.

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Outline

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- Motivation and purpose of this work
- Details of the in-process screening technique
- Annealing of screening damage by high-temperature treatment after screening
- Acceleration models for early failures due to oxide TDDB and the screening conditions
- Results of application to the 0.8 μ m technology
- Summary and conclusions

WLR5-2

WLR5-1

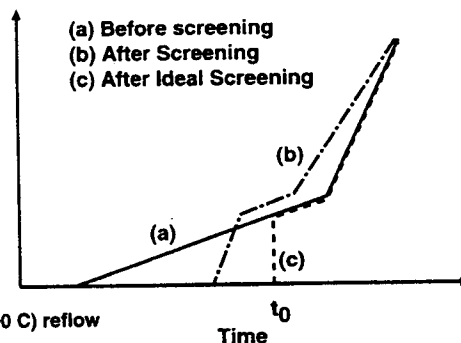
Issues in standard burn-in method

- For logic devices, it is impossible to activate and stress every gate oxide in a realistic time
- Limitation to voltage acceleration due to transistor breakdown voltage
- Reduction in the life time of surviving gate oxides, since no damage recovery process is available after burn-in
- These come from
 - Burn-in stress on functional circuits (products) where metallization has been completed

WLR5-3

Basic idea behind in-process wafer-level screening

- Ideal screening method
 - Stress to all usable gate oxides on a chip
 - Any high voltage acceleration
 - Recovery process from screening damage given to the surviving oxides
- Voltage stress before metallization
 - Free from transistor breakdown since no wiring of source and drain
 - Damage can be annealed by high temp. (> 600 C) reflow process



WLR5-4

What's new in this work

- Feasibility study appeared in previous work:
 - J. C. King, W. Y. Chan, and C. Hu, "Efficient Gate Oxide Defect Screen for VLSI Reliability," IEDM, 1997
 - This paper is very preliminary and does not have any discussion on implementation to CMOS process
- In this work, the in-process screening has been implemented to CMOS process for the first time and effectiveness of this method is demonstrated

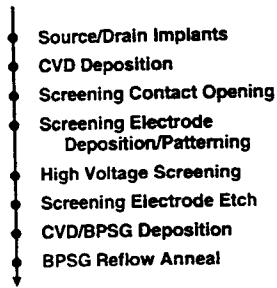
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Details of the in-process screening

- Two key processes are added to the standard CMOS process for the simultaneous screening of all usable gate oxides
 - Contact opening for the screening electrode to all poly-Si gates
 - Patterning of the screening electrode to connect all gates in parallel

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Process flow of the in-process screening



- high temperature annealing, e.g., reflow of the BPSG film at 900C is available for screening damage recovery
- The position of the screened chips on the wafer is recorded for later identification after processing

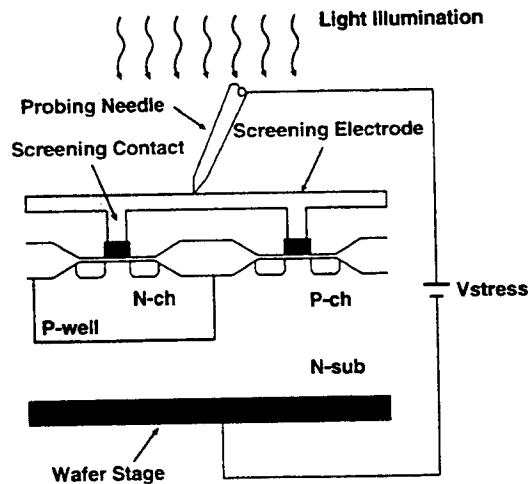
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Screening method

- For CMOS devices before metallization
 - Available electrode for voltage force to the gate oxides are the screening electrode and the back side of the wafer
 - If PMOS is in inversion, then NMOS is in accumulation, and vice versa
 - Need enough inversion carriers for expected oxide field
- Inversion carriers can be generated by light illumination over the wafer

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Schematic illustration of the device under screening

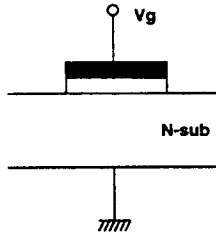
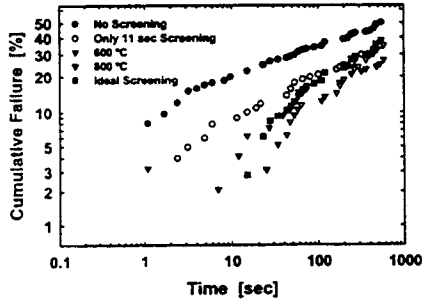


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Screening damage recovery by high-temperature anneal

MOS cap : $T_{ox}=9.7nm$, Gate Area = $10mm^2$
 Screening stress: $8MV/cm$, 11sec, room temp

$$F(\text{Ideal screening}) = F(\text{no screening}) - F(<11\text{sec})$$



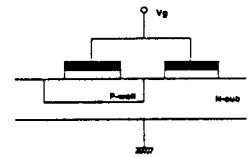
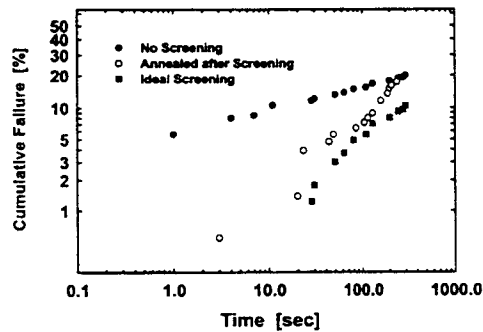
600C is enough to recover screening damage

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Screening damage recovery by high-temperature anneal (cont.)

MOS cap with p-well/n-sub: $T_{ox}=15nm$, Gate Area = $6.5mm^2$
 Screening stress: $8MV/cm$, 11sec, room temp
 Anneal after screening: $800C$

$$F(\text{Ideal screening}) = F(\text{no screening}) - F(<11\text{sec})$$

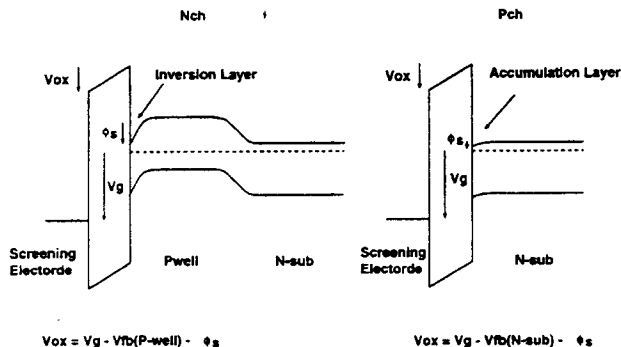


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Determination of the screening voltage

Band diagram and oxide voltage of PMOS and NMOS under light illumination for p-well/n-sub CMOS

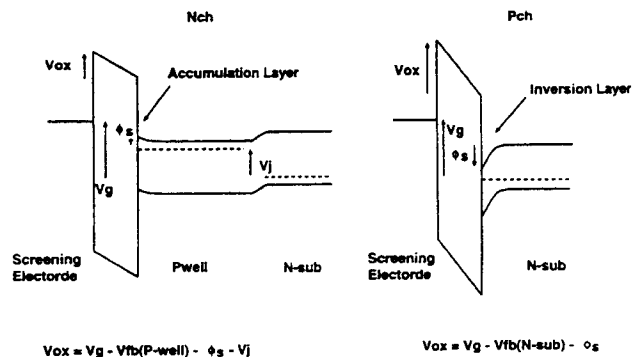
(1) $V_g > 0$



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Determination of the screening voltage (cont.)

(2) $V_g < 0$



WLR5-13

Determination of the screening voltage (summary)

| | PMOS | NMOS |
|--------|-----------------------------|------------------------------------|
| Vg > 0 | Vg - Vfb(N-sub) - φs(N-sub) | Vg - Vfb(Pwell) - φs(P-well) |
| Vg < 0 | Vg - Vfb(N-sub) - φs(N-sub) | Vg - Vfb(P-well) - φs(P-well) - Vj |

For channel concentration of $1 \times 10^{15} \text{cm}^{-3}$

| | PMOS | NMOS |
|--------|----------|---------------|
| Vg > 0 | Vg - 0.1 | Vg - 0.1 |
| Vg < 0 | Vg + 1.2 | Vg + 1.2 + Vj |

Therefore, for N-sub/P-well structure, it is possible to apply the same oxide voltage to both PMOS and NMOS if $V_g > 0$

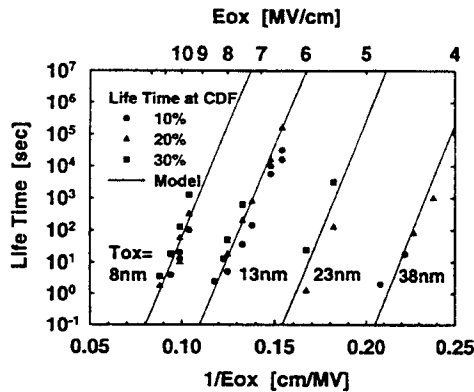
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Voltage acceleration model for early TDDB failures

MOS capacitors: $T_{ox} = 8\text{nm} - 38\text{nm}$ Gate Area = 10mm^2

Early failures: life time at 10%, 20% and 30%

$TTF \sim \exp(320/E_{ox}[\text{MV/cm}])$

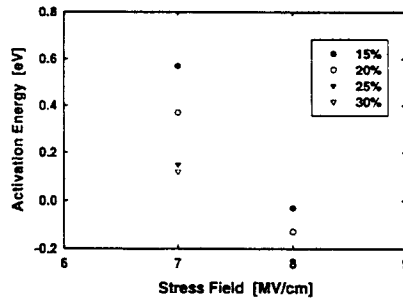


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Temperature acceleration model for early TDDB failures

MOS capacitors: $T_{ox} = 15\text{nm}$ Gate Area = 6.5mm^2

Early failures: life time at 15%, 20%, 25% and 30%



The data shows that E_a depends on the stress field consistent with the reference, e.g. K. C. Boyko and D. L. Gerlach in 1989 IRPS

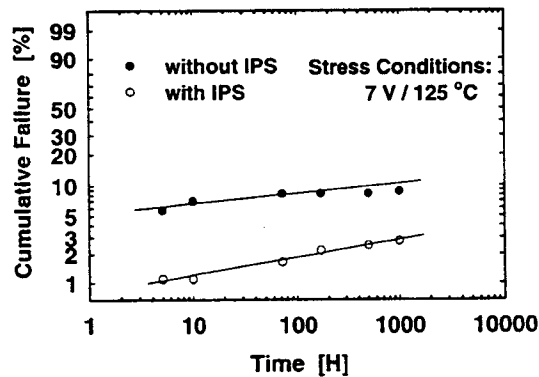
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Application to 0.8 μ m CMOS logic

- **Process:**
 - p-well/n-sub structure
 - $T_{ox} = 15\text{nm}$
 - Double-level metallization
- **Screening stress conditions**
 - $E_{ox} = 5.8\text{MV/cm}$, Time = 5sec, T = room temp
- **The stress conditions are equivalent to:**
 - $E_{ox} = 7\text{V}/15\text{nm} = 4.67\text{MV/cm}$, Time = 10H, T = 125C
 - (these are typical burn-in conditions for 0.8 μ m CMOS logic)
 - for $E_a = 0.3\text{eV}$ at this stress field (K. C. Boyko and D. L. Gerlach in 1989 IRPS)

WLR5-17

Results on the in-process screening



Early gate oxide failures are obviously reduced by the in-process screening

WLR5-18

Summary and conclusions

- A novel wafer-level in-process screening method has been developed:
 - Stress to all usable gate oxides at the same time can be done, which is impossible in the conventional burn-in
 - High temperature treatment after screening can be used to recover screening damage in surviving oxides
 - Any high voltage can be used for screening stress
- This method has been applied to 0.8 μ m CMOS technology, and it has been demonstrated that this method is very effective for reducing early gate oxide failures

WLR5-19