IEEE/Integrated Reliability Workshop
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PROGRAM ANNOUNCEMENT!

You are cordially invited to participate in the 2006 Integrated Reliability Workshop. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. Here you will closely interact with your peers at moderated discussion groups, open poster sessions, technical sessions, tutorials, and special interest groups. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learning and discussions. You should come away from the workshop intellectually stimulated and refreshed!

Major Technical Themes

The Integrated Reliability Workshop covers a wide and well-balanced spectrum of pressing reliability challenges, preparing attendees for reliability problems at hand and those to come. The focus points reflected by this year's program include gate dielectric reliability, transistor reliability including NBTI and hot carrier aging, interconnect reliability covering metal line and via electromigration and stress migration, wafer level reliability, passive reliability for mixed signal, memory reliability, as well as product reliability.

This year's workshop features eight tutorials by world leading experts. Topics include dielectric reliability, NBTI, interconnect reliability including Cu electromigration and integrating high-k dielectrics into BEOL process, memory reliability, imager and sensor reliability, new reliability challenges, and qualification strategy. The tutorials will be presented in two parallel sessions on Monday afternoon.

Our keynote on Tuesday morning will be given by Dr. Jose Antonio Maiz, Intel Fellow, Director of Logic Technology Quality & Reliability, Intel Corporation on "Reliability Challenges: Preventing Them from Becoming Limiters to Technology Scaling".

As usual, all authors, including the tutorial speakers and the keynote speaker will be available for discussions during the workshop. Ample time is scheduled for one-on-one exchanges, organized discussion groups, the popular and productive SIGs (Special Interest Groups), inter-session breaks, and poster sessions where all attendees are encouraged to display a poster and discuss their most recent work, ideas, and results. Wednesday afternoon is available for recreation with fellow attendees, a great way to become more acquainted with your colleagues.

Overall this represents an exciting, well-balanced program that addresses the needs and interests of today's reliability engineers for the benefit of their company. We invite you to tell your colleagues and your managers about this year's IIRW. Make a point to let them know that both the attendees and their organizations gain from this investment in learning, which helps in dealing with today's challenges and preparing for tomorrow's.

'06 Workshop Features:

- ✶ **Keynote: Reliability Challenges: Preventing them from Becoming Limiters to Technology Scaling—Dr. Jose Antonio Maiz, Intel Fellow, Director of Logic Technology Quality & Reliability, Intel Corporation**
- ✶ **Group Discussions**
  - Gate Oxide / High-k Reliability
  - NBTI
  - Interconnect Reliability
  - Product/Circuit Reliability
- ✶ **8 Tutorials**
  - SiON Gate Dielectric Reliability
  - NBTI in MOS Devices
  - Cu Electromigration
  - Integrating High-K Diel. into BEOL Process
  - Phase Change Memory Reliability
  - Image Sensors Reliability
  - Reliability New Challenges
  - Reliability Qualification Strategy
- ✶ **28 Technical Presentations on:**
  - Interconnect Reliability
  - Ultra-Thin Oxides / High-k Reliability
  - NBTI/Hot Carrier Aging
  - Capacitor & Resistor Rel. for Mixed Signal
  - Memory Reliability
  - Product Reliability
  - Wafer Level Reliability
- ✶ **24 Refereed Posters + Open Posters**
- ✶ **Special Interest Groups**

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–over–

KEYNOTE

Reliability Challenges: Preventing Them from Becoming Limiters to Technology Scaling

Jose Antonio Maiz, *Intel Fellow, Technology and Manufacturing Group, Director of Logic Technology Quality & Reliability, Intel Corporation*

Aggressive technology scaling continues as projected by Moore's Law and has not shown signs of slowing down to date. The International Technology Roadmap for Semiconductors (ITRS) projects major challenges for the coming decade including the very real possibility that, along with power, reliability may become a limiter. Fundamental changes in key materials, transistor architectures, and interconnects are compounded by interactions with design, changes in computing architecture, and the exploration of exotic technologies as potential replacements/ complements to the very successful planar CMOS transistor.

In this address, an analysis of the key technology trends relevant to reliability as well as key reliability trends with a potential to slow down technology scaling will be discussed along with key concerns for some of the proposed exotic options. This analysis will allow an exploration of the options, opportunities for research, and directions that will contribute to removing reliability as a limiter or, at a minimum, to minimize its impact.

TUTORIALS

Chair: Guoqiao Tao, Philips

Reliability of On-The-Shelf Stored Image Sensors

Albert J.P. Theuwissen, Dalsa

Tutorial A1, Monday, 1:30-2:30 p.m. (Angora Room)

An aging effect in solid-state image sensors is studied: the generation of hard errors resulting in hot spots or white pixels. These effects manifest themselves as an increase in dark current, a loss in transfer efficiency (in the case of CCDs) and in extra "hot spots". The effects even occur in sensors that are stored on the shelf. It is well known in the imaging community that image sensors are subject to a degradation effect due to radiation. For instance, devices intended for space application are fabricated in special processes so that the sensors can withstand radiation or to make them radiation-hard. The question is whether similar effects are also responsible for the creation of hot pixels during normal on-the-shelf storage of image sensors. Simply storing imaging devices on the shelf does indeed result in a few extra hot spots in the picture taken at a later time. It is important to point out that these hot spots or leaky pixels are permanent. They are not a soft error, in the sense that a high-energy particle is absorbed in the silicon, generates a cloud of charge carriers and after the next image all effects are gone. The effects investigated in this study are hard errors: once they are created, they remain present in the imagers. This tutorial describes experiments that are conducted to prove that the main origin can be found with neutrons that are part of terrestrial cosmic rays.

Phase Change Memory Reliability

Su Jin Ahn, Samsung

Tutorial B1, Monday, 1:30-2:30 p.m. (Cathedral Room)

Phase Change Memory (PRAM) is considered to be one of the viable candidates for the next generation to solve the problems and intrinsic scaling limits of conventional nonvolatile memory. Recently, there have been great advances in PRAM development including new phase change materials, various device structures, process technology innovations, and device designs. This tutorial will introduce operation principles of PRAM exploiting new memory material called chalcogenide and then report the reliability considerations to become commercial products. The reliability issues are disturbance immunity, cycling endurance, data retention and degradation related to back-end process. The experiments have been performed by using 256Mb-density device and the observed degradation modes and underlying physical mechanism have been discussed.

New Challenges and Requirements to Reliability Research and Development in Semiconductor Technology Evolution

Yi Ma, Applied Materials

Tutorial A2, Monday, 2:30-3:30 p.m. (Angora Room)

Semiconductor technology has made significant progress in the past decade. Device dimension has been down scaled to sub-nanometer range. The progress is primarily driven by market force, products with higher performance and lower cost. In the mean time, the semiconductor product market has shifted to more diversified consumer products versus conventional enterprise products. The trend added more complexity and uncertainty of technology direction, the pressure to deliver product to market on time has been heightened. As a result, numerous new materials, new process integration schemes and new design concepts have been developed and implemented to meet the technology demands. Reliability research and development has been significant part of the vicious technology progress. In this talk, I'll explore challenges and requirements Reliability community will face in the coming technology generations from a technology engineering point of view. I'll discuss how technology development cycle and cost can be reduced if impacts of material and process integration on reliability are understood at early stage of technology development. I'll also explain why developing new methodologies and establishing new reliability standards are critical to early technology adoption by design community and market place.

Strategy of Future Reliability Qualification

Andreas Preussger, Infineon Technologies

Tutorial B2, Monday, 2:30-3:30 p.m. (Cathedral Room)

The most efficient qualification strategy has become a major part of successful development of products and technologies. The boundary conditions for reliability have become tighter and the dependency between product design, technology and reliability performance has been increased. The discussion on this topic has now reached the community working on standards and guidelines. Qualification standards from the old age work with lists of stress tests that have to be performed to demonstrate the reliability of a product. They give fixed test times and gating criteria like "no fail out of a sample of some ten parts" to be tested mostly in a black box approach, where the failure mechanism is not known because the test ends typically before the first failure is activated.

One example of a standard describing such a procedure is the AEC-Q100, a stress test driven approach which has been created by the Automotive Electronic Council (AEC). It describes a stress test driven qualification approach. Similar standards exist from JEDEC and Telcordia. These standards were needed to improve the quality level at IC manufacturers, their suppliers and the OEMs which were in the range of percents in the late seventies.

Today's products and especially new technologies following the Technology Roadmap are facing certain new challenges that are not covered by old stress test driven qualification approaches.

Complexity of technologies and products is increasing per technology node and per product generation. The products are covering more functions within one IC. This improving can only be achieved by better performance of the technologies used to build the products. These improvements on the technology side can only be achieved by changing the materials with an increasing frequency which means that the rate of introduction of new materials to be introduced as solutions for upcoming problems will be dramatically increasing. Therefore the time for development, implementation and learning with these new materials becomes shorter and shorter. In this context the term qualification has to be redefined.

The development from the old stress based approach to modern strategies like knowledge based qualification using robustness validation are presented in the tutorial together with some application examples how robustness of products could be measured based on technology. Application areas which do not follow these new approaches run the risk to loose contact to the state-of-art technologies.

The present example of via reliability is used to explain what methodologies could be used to find the trade off between performance, design and reliability. Many design challenges are linked to reliability. Tools offered by EDA vendors are now able to do design optimization with respect to yield and reliability as an integrated part of the standard design flow. The integration of the reliability tools is typically done in a partnership between EDA vendor and chip manufacturer. Examples will be presented.

SiON Gate Dielectric Reliability

Paul Nicollian, TI

Tutorial C1, Monday, 4:00-5:00 p.m. (Angora Room)

SiON films continue to be the choice gate dielectrics for high performance CMOS. Driven by the relentless race to achieve increasingly aggressive performance targets, the continued scaling of electrical thickness is now compounded by the slowing of voltage scaling. This has resulted in the erosion of reliability margins to razor thin levels, requiring an increasingly sophisticated understanding of the degradation physics of these films. In this tutorial, we will discuss the advancements and issues in breakdown mechanisms and lifetime modeling that is important for enabling deeply scaled SiON films to meet challenging high performance reliability requirements.

Current Challenges in Cu Electromigration Reliability

Christine Hau-Riege, AMD

Tutorial D1, Monday, 4:00-5:00 p.m. (Cathedral Room)

In today's integrated circuit (IC), more than a kilometer of metal interconnects are required to build a single microprocessor, so that many billions of metal segments exist in each IC. These metal segments are a significant reliability concern due mainly to electromigration. This concern increases with each new generation of microprocessor, which requires the use of a larger number of narrower interconnects, stressed at increasing current densities. This tutorial will address the basics of Cu electromigration and current routes for improved reliability.

The Negative Bias Temperature Instability in MOS Devices

Sufi Zafar, IBM

Tutorial C2, Monday, 5:00-6:00 p.m. (Angora Room)

Negative bias temperature instability (NBTI) has become an increasingly important reliability issue for advanced CMOS technology. In the present tutorial, the experimental and theoretical understanding of NBTI will be reviewed. This

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2006 IEEE INTERNATIONAL INTEGRATED RELIABILITY WORKSHOP
PROGRAM

MONDAY, October 16

Please have lunch before arriving at the camp; no lunch will be served at the camp.

1:00 – 6:00 p.m. Registration: Pick up badges & handout (*Lodge Lounge*) Discussion Group and SIG sign up; Poster preparation

1:00 – 8:00 p.m. Lodge check-in. Get room assignment (prearranged) & room key. (If physically challenged please notify desk of special needs.)

1:30 – 6:00 p.m. **Tutorials** (parallel sessions): Chair: *Guoqiao Tao, Philips & Rolf Geilenkeuser, AMD*

	Angora Room	Cathedral Room
1:30–2:30	A1: Image Sensor	B1: Phase Change Memory
2:30–3:30	A2: Reliability Challenges	B2: Qualification Strategy
3:30–4:00	Break (poster preparation)	
4:00–5:00	C1: Dielectrics	D1: Cu Electromigration
5:00–6:00	C2: NBTI	D2: High-k in BEOL

6:15 – 7:30 p.m. DINNER, *(Dining Room)* authors: dine with your session chair

7:30 – 10:30 p.m. Announcements and Poster Session & Mixer *(Cathedral Room)*—Poster Session Chair: *Sylvie Bruyère, STMicroelectronics*

TUESDAY, October 17

7:00 – 8:00 a.m. BREAKFAST *(Dining Room)*

8:00 – 8:15 a.m. Welcome & Introduction: John Conley, General Chair *(Angora Room);* Technical Program Overview: Yuan Chen, Technical Program Chair

8:15 – 9:15 a.m. Keynote: Reliability Challenges: Preventing Them from Becoming Limiters to Technology Scaling – Dr. Jose Maiz, Intel Fellow, Director, Logic Technology Quality & Reliability, Intel

9:15 – 9:25 a.m. Break

9:25 –11:30 a.m. **SESSION #1: NBTI,** Chairs: Yuan Chen, JPL and Bill Knowlton, Boise State University

1.1 On the impact of the NBTI recovery phenomenon on lifetime prediction of modern p-MOSFETs – C. Schlunder, W. Heinrigs, W. Gustin, H. Reisinger, Infineon

1.2 Modeling of dispersive transport in the context of negative bias temperature instability – T. Grasser, W. Gos, Institute of Microelectronics, B. Kaczer, IMEC

1.3 Identifying negative bias stressing interface trapping centers in metal gate hafnium oxide field effect transistors using spin dependent recombination – C.J. Cochrane, P. Lenahan, J.P. Campbell, Penn State Univ, G. Bersuker, P. Lysaght, SEMATECH, A. Neugroschel, Univ. of Florida

1.4 Effects of delay time and AC factors on negative bias temperature instability of PMOSFETs – P. Juan, M Chen, P. Juan, and K. Su, UMC

1.5 On-the-fly bias pattern as a tool to study CMOS degradation – CR Parthasarathy[1,3], M. Denais[1], V. Huard[2], C. Guerin[1], G. Ribes[1], M. Rafik[1], W. Baks[2], F. Perrier[2], D. Roy[1], E. Vincent[1], A. Bravaix[3] [1]STMicroelectronics, [2]Philips Semiconductors, [3]L2MP–ISEN

11:30 – 12:00 p.m. Group Picture

12:00 – 1:00 p.m. LUNCH, *Dining Room*

1:10 –2:25 p.m **SESSION #2: Interconnects**, Chairs: Harry Schafft, NIST and Timothy Sullivan, IBM

2.1 Bias stress induced conduction mechanism evolution in silica based inter-metal dielectrics – Y. Li, G. Groeseneken, K. Maex, Zs. Tõkei, IMEC

2.2 Dynamics of resistance evolution during electromigration stress – X. Federspiel, L. Doyen, Philips, D. Ney, V. Girault, STMicroelectronics

2.3 Stress migration phenomena in narrow copper lines – H. Matsuyama, T. Kouno, T. Suzuki, M. Shiozu, H. Ehara, S. Otsuka, T. Hosoda, T. Nakamura, Y. Mizushima, K. Shono, M. Miyajima, Fujitsu

2:25 – 3:15 p.m. **SESSION #3: C&R for Mixed Signal**, Chairs: Timothy Sullivan, IBM and Harry Schafft, NIST

3.1 Impact of TiN plasma post-treatment on alumina electron trapping – A. Bajolet[1,2], S. Bruyère[1], M. Proust[1], L. Montès[2], G. Ghibaudo[2], [1]STMicroelectronics, [2]IMEP

3.2 Constant-current stressing of SiCr-based thin film resistors: Initial "wearout" investigation – R. Brynsvold, K. Manning, Analog Devices

3:15 – 3:35 p.m. Break

3:35 – 5:40 p.m. **Session #4: Transistor Reliability**, Chairs: Andreas Martin, Infineon & Marie Ruat, STMicroelectronics

4.1 Effect of photo misalignment on N-LDMOS hot carrier device reliability – D. Brisbin, P. Lindorfer, P. Chaparala, National Semiconductor

4.2 Ultra-fast measurements of Vth instability in SiC MOSFETs due to positive and negative constant bias stress – M. Gurfinkel[1], J. Suehle[2], J. Bernstein[1], Y. Shapira[1], A.J. Lelis[3], D. Habersat[3], N. Goldsman[1] [1]University of Maryland; [2]NIST; [3]ARL

4.3 Effect of self-heating on HCI lifetime prediction in SOI technologies – J.M. Roux[1], X. Federspiel[2], D. Roy[1] [1]STMicroelectronics, [2]Philips

4.4 Reliability characterizations of a 150GHz Ft/Fmax Si/SiGeC heterjunction bipolar transistor under reverse, forward and missed-mode stress – M. Ruat[1,2], J. Bourgeat[1], M. Marin[1], G. Ghibaudo[2], N. Revil[1], G. Pananakakis[2] [1]STMicroelectronics; [2]IMEP

4.5 Impact of hot carrier degradation modes on I/O nMOSFETS aging prediction – C. Guerin[1], V. Huard[2], A. Bravaix[3], M. Denais[1] [1]STMicroelectronics; [2]Philips; [3]L2MP-ISEN

6:00 – 7:30 p.m. DINNER, *Dining Room*

7:30 – 8:30 p.m. Poster Session & Mixer: Chair: *Sylvie Bruyère, STMicroelectronics*

8:30 – 9:30 p.m. Discussion Groups: Chair: *Pat Lenahan, Penn State Univ.* (One hour parallel sessions for each topic)
Attendees are to participate in one of the groups: 1. Gate Oxide / High-k; 2. NBTI; 3. Interconnects; or 4. Product/Circuit Reliability

9:30 – 10:30 p.m. Individual SIG Meetings (to be announced at camp)

WEDNESDAY, October 18

7:00 – 8:00 a.m. BREAKFAST *(Dinning Room)*

8:00 – 8:10 a.m. Announcements, *(Angora Room)*

8:10 – 9:50 a.m. **SESSION #5: MEMORY RELIABILITY**, Chairs: Bill Tonti, IBM and Sufi Zafar, IBM

5.1 Reliability issues related to Fast Charge Loss Mechanism in Embedded Non Volatile Memories – P. Mora, S. Renard, G. Bossu, P. Waltz, STMicroelectronics, G. Pananakakis, G. Ghibaudo, IMEP

	5.2 Flash Oxide Scalability Model and Impact of Program/Erase Method – A. Haggag, P. Kuhn, P. Ingersoll, C. Li, M. Niset, T. Harp, A. Hoefler, D. Burnett, K. Baker, K. Chang, Freescale Semiconductors
	5.3 Experimental Study of Temperature Dependence of Program/Erase Endurance of Embedded Flash Memories with 2T-FNFN Device Architecture – G. Tao, H. Chauveau, S. Nath, Philips Semiconductors
	5.4 A Critical Failure Source in 65nm-MLC NOR Flash Memory Incorporating Co-Salicidation Process – J. Han, B. Lee, J. Han, S. Sim, C. Park, and K. Kim, Samsung
9:50 – 10:10 a.m.	Break
10:10 – 11:00 a.m.	Session #6: Products Reliability, Chairs: Al Strong, IBM & Andreas Preussger, Infineon
	6.1 Study of Electrically Programmable Fuses through Series of I-V – H. Suto, S. Mori, M. Kanno, N. Nagashima, Sony
	6.2 NiSi Polysilicon Fuse Reliability in 65nm Logic CMOS Technology – B. Ang, S. Tumakha, J. Im, S. Paak, Xilinx
11:00 – 11:50 a.m.	Session #7: Wafer Level Reliability, Chairs: Andreas Preussger, Infineon & Al Strong, IBM
	7.1 Fast productive WLR characterization methods of plasma induced damage of thin and thick MOS gate oxides – A. Martin[1], C. Siol[2], C. Schlünder[1], U. Schwalke[2] [1]Infineon Technologies; [2]Technical Univ of Darmstadt
	7.2 Practical Considerations for Wafer-Level Electromigration Monitoring in High Volume Production – O. Aubel, AMD, T.D. Sullivan, D. Massey, T.C. Lee, T. Merrill, S. Polchlopek, A. Strong, IBM
12:00 – 1:30 p.m.	LUNCH (*Dining Room* — Take out Lunch bags available)
1:30 – 5:00 p.m.	Open The afternoon is free for discussion, hiking & other recreation
5:00 – 6:00 p.m.	Mixer & Poster Session: Chair: *Sylvie Bruyère, STMicroelectronics*
6:00 – 7:30 p.m.	DINNER, *Dining Room*
7:30 – 8:30 p.m.	Late News Paper Session:
8:30 – 9:30 p.m.	Discussion Groups: Chair: *Pat Lenahan, Penn State Univ.* (One hour parallel sessions for each topic) Attendees are to participate in one of the groups: 1. Gate Oxide / High-k; 2. NBTI; 3. Interconnects; or 4. Product/Circuit Reliability
9:30 – 10:30 p.m.	Individual SIG Meetings (to be announced at camp)

THURSDAY, October 19

7:00 – 8:00 a.m.	BREAKFAST (*Dining Room*)
8:15 – 8:30 a.m.	Announcements, *(Angora Room)*
8:30 – 10:35 p.m.	Session #8: High-k Dielectrics, Chairs: John Conley, Sharp & John Suehle, NIST
	8.1 Spatial probing of traps in ALD HfO_2/SiO_2 stacks using low frequency noise characteristics – H. Xiong, J. Suehle, NIST
	8.2 New Insight on the origin of Stress Induced Leakage Current for SiO_2/HfO_2 dielectric stacks – M. Rafik, G. Ribes, S. Kalpat, STMicroelectronics, G. Ghibaudo, IMEP
	8.3 Fast and slow charge trapping/detrapping processes in high-k nMOSFETs – D. Heh, C. D. Young, R. Choi, and G. Bersuker, Sematech
	8.4 Influence of Stress-Induced-Leakage-Current on Reliability of $HfSiO_x$ with EOT>1.5nm and TiN Gate – S. Jakschik[1], Th. Kauerauf[2], R. Degreave[2], Y. N. Hwang[3], R. Duschl[4], M. Kerber[1], A. Avellan[4], S. Kudelka[4] [1]Infineon; [2]IMEC; [3]Samsung; [4]Qimonda
	8.5 Leakage current variation with time in Ta_2O_5 MIM and MIS capacitors – J-P. Manceau[1,2], S. Bruyere[1], S. Jeannot[1], A. Sylvestre[2], P. Gonon[3] [1]STMicroelectronics; [2]LEMD; [3]LTM
10:35 – 11:00 a.m.	Break (Time to check out!)
11:00 – 12:00 p.m.	DG Summary / SIG Report / Wrap-up
Noon – 1:20 p.m.	LUNCH, *(Dining Room)* & then the Workshop Ends— Attendees must leave the Stanford Sierra Camp unless attending JC14.2
2:00-2:30 p.m.	JEDEC 14.2 Introductions/agendas/minutes and subcommittee sessions
2:30-6:00 p.m.	JEDEC subcommittee sessions: Device, Dielectric, Interconnect, Fab Spec

FRIDAY, October 20

7:00-8:00 a.m.	Breakfast
8:00-10:30 p.m.	JEDEC subcommittee sessions continuation
10:30-11:00 a.m.	Break and checkout
11:00-12:00 p.m.	JEDEC Summaries & Wrap-up
12:00-1:00 p.m.	Lunch and leave camp

2006 IIRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 19-20)

Meeting registration automatically includes a room reservation.

(Please type, print or attach business card)

NAME: ______________________________
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For cabin assignments: ❑ male ❑ female

❑ Address is HOME

❑ Please check here if you do not wish to receive mail other than from IIRW & IRPS

❑ Please check here if physically challenged and you require any auxiliary aids or services. Please call (315) 339-3968.

❑ Will bring poster. Title: ______________________

I am interested in the following Discussion Group(s):

❑ Gate Oxide/High-k; ❑ NBTI; ❑ Interconnects; ❑ Product Reliability;

❑ My Suggestion ______________________

Method of Payment: ❑Check: Make checks payable to: **2006 IEEE/IIRW**

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ADVANCE REGISTRATION FEES

IEEE Member (incl. mem#__________) **$1125*** ________

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IEEE STUDENT**(mem#__________) **$825*** ________

After 6-Oct-06 add late fee $100 ________

** Includes workshop attendance & handout materials, tutorial attendance, 3 nights lodging (Monday—Wednesday) 9 meals (dinner Monday— lunch Thursday), Final Workshop Report with CD.*

***To promote student involvement at IIRW, we will be offering a reduced registration fee of $825 to the **first 15 students** who register . Students accepting the discount must be either IEEE member, or join the IEEE as a student member.*

EXTRA COPIES of Workshop?

Final Report (printed) Qty:__ x **$80** ________

Final Report (CD).... Qty.___x **$80** ________

Final Report (printed & CD) Qty:__ x**$130** ________

JC-14.2 Mtg. accommodations*** **$260** ________

**** Includes 1 night lodging (Thursday), 3 meals (dinner Thursday— lunch Friday)*

TOTAL REMITTED $ ____________

No wire transfers Cancellation fees: $50 after Sept. 22 ; full fee after Oct. 6

Send this completed form and payment to: IIRW Registration; P.O. Box 308; Westmoreland, NY 13490 Paying by credit card... fax to 315-336-9134
Questions? becky@sar101.com or 315-339-3968 or web site: http://www.iirw.org

(TUTORIALS cont. from page 2)
tutorial will be organized as follows: Section I will review the experimental observations which characterize NBTI. This section will discuss the dependence of NBTI on stress conditions including measurement methodologies. The dependency of NBTI on process conditions will also be discussed. Section II will review various models, comparing the various theories proposed for NBTI. Section III will discuss the practical implications of NBTI, including the performance degradation of circuits. Section IV will discuss the implications for new gate-stack materials. Finally, Section V will summarize some of the many open questions.

Reliability Aspects of Integrating High-K Dielectrics into Back-End-of-Line (BEOL) Process Technology

Tom Remmel, James Walls and Douglas Roberts, Freescale Semic.

Tutorial D2, Monday, 5:00-6:00 p.m. (Cathedral Room)

The demand to provide increased integrated circuit functionality at continually decreasing prices is driving the integration of more and more components on-chip. This on-chip migration now includes the incorporation of passive elements directly into the integrated circuit process flow; elements that were previously resident off-chip. Common integrated passive devices include discrete components such as inductors, capacitors and resistors, but could also include resonators, filters, and even optical components. Because of their nature, these devices are usually integrated within or on top of the multi-level metallization. Several of these devices are fabricated using high dielectric constant (high-K) materials. Integrating these materials on-chip presents an array of challenges, including multi-dimensional trade-offs between materials selection, unit process definition, insertion point into the process flow, electrical performance, defectivity, yield and reliability. This paper will focus on the opportunities and trade-offs of integrating high dielectric constant materials into the back-end-of-line process. Throughout the development process, reliability is the key metric which drives many of the decisions.

DISCUSSION GROUPS

Chair: Pat Lenahan, Penn State University

The evening discussion group program is regarded as a favorite highlight of the workshop experience. Attendees will have a choice of two areas on Tuesday and Wednesday evenings. The topics to be discussed will be at the discretion of those participating in the group. Each group is assigned a pair of leaders who have extensive experience with the area and will help to guide the discussion. Everyone is encouraged to bring along data and/or ideas to share on topics that are of particular interest. As we get closer to the date of the workshop, we will be surveying registered attendees so that we may prepare relevant discussion outlines to be distributed at the camp. This year's discussion areas and leaders are:

1. *Gate oxide / High-k:*
Chad Young, Sematech and Evgeni Gusev, Qualcomm

2. *NBTI*: Sufi Zafar, IBM and Tomasz Brozek, PDF Solutions

3. Interconnects: Timothy Sullivan, IBM

4. Product/Circuit reliability:
Andrew Turner, IBM and Mark Porter, Medtronics

SPECIAL INTEREST GROUPS

Chair: Pat Lenahan, Penn State University

A Special Interest Groups (SIGs) is a collaborative working team focused on one compelling topic of mutual interest. The SIG program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. For more information on SIGs, please see http://www.iirw.org/06/06SIG.html.

REFEREED & OPEN POSTER SESSIONS

(Monday, Tuesday, and Wednesday Evenings)

Chair: Sylvie Bruyère, STMicroelectronics

In addition to our refereed poster sessions featured below, all attendees have the opportunity to present a poster to communicate and discuss their ideas and newest results on technical projects or issues. Please indicate in the space provided on the registration form your intention to bring a poster. A poster display board (32" x 40" or 81 cm x 100 cm) will be reserved for you. Your work should be in landscape format on 8½ x 11" or A4 paper with a maximum of twelve pages. This is a great opportunity for you to share your work with your peers. Also feel free to bring last minute results, board space will be found for you.

IIRW 2006 Refereed Posters:

P1 Residual resistivity model and its application, L. Doyen et al., Philips

P2 Ultra-fast NBTI monitoring and end-of-life projection, C. Wang et al., UMC

P3 Impact of monitoring voltage on the lifetime extrapolation during the accelerated degradation tests, F. Duan and S. Cooper, AMD

P4 Oxide reliability: a new methodology for reliability evaluation at parametric testing, R. Bottini et al., STMicroelectronics

P5 NBTI degradation and its impact for voltage controlled oscillators, E. Xiao et al., Univ. of Texas at Arlington

P6 Temperature effect and breakdown mechanism in ultra-thin gate oxide, C.-L. Lin et al., UMC

P7 Preliminary study of the breakdown strength of TiN/HfO_2/SiO_2/Si MOS gate stacks, R. Southwick et al., Boise State Univ.

P8 Cryogenic performance & reliability of GaAs CHFETs, R. Leon & Y. Chen, JPL

P9 Lithography CD variation effects on LFNDMOS transistor hot carrier degradation, M. Thomason et al., AMI Semiconductor

P10 Product reliability trends, derating considerations and failure mechanisms with scaled CMOS, M White et al., JPL

P11 Modeling of bias stress-induced instability of SiC MOSFETs, S. Potbhare et al., Univ. of Maryland

P12 Temperature effects on the hot-carrier induced degradation of pMOSFETs, S. Chen et al., National Taipei Univ. of Technology

P13 ESD robustness of 40-V CMOS devices with/without drift implantation, W. Chang et al., National Chiao-Tung Univ.

P14 Burn-in acceleration considerations in 90nm system LSI, N. Wakai et al., Toshiba

P15 Reliability of strain-Si FPGA product fabricated by novel ultimate spacer process, Y.H. Luo et al., Xilinx

P16 The correlation of interface defect density and power-law exponent factor on ultra-thin gate dielectric reliability, Y.C. Yang et al., UMC

P17 Fast prediction of gate oxide reliability – Application of the cumulative damage principle for transforming V-ramp breakdown distributions into TDDB failure distributions, A. Aal, ELMOS Semiconductor AG

P18 Ultra-thin gate oxide lifetime projection and degradation mechanism beyond 90 nm CMOS technology, C.-L. Lin et al., UMC

P19 Impact of error correction code and dynamic memory reconfiguration on high reliability/low cost server memory, C. Slayman et al., Sun Microsystems

P20 Blowing polysilicon fuses: what conditions are best, Y. Li and A. Tang, Analog Devices

P21 A new mechanism of poly-silicon crater defect induced from Al particle charging effect during water rinse in oxide patterning process, L.J. Duan et al., Philips

P22 Analysis method of characterizing Isb failure of multiple times programming flash IP, L.F. Wen, J.T. Hsu, and C.H. Chen, TSMC

P23 Wafer reliability evaluation for InGaAsP devices, D.Verbitsky, Alefa

P24 Surface roughness enhanced current in defectively stressing double-poly capacitors, L. Sheng et al., AMI Semiconductor

JEDEC 14.2 Meeting. The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is $260.00, which includes Thursday night dinner and lodging, and Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558, see www.jedec.org, or contact Al Strong (astrong@us.ibm.com), JC-14.2 Chair, at (802) 769-1326.

More Information. We expect an exciting workshop again this year. Your active participation in the many workshop activities and your active contributions to the technical discussions are key ingredients for the value of the workshop for all attendees. If you have additional questions, please contact either: me, the Technical Program Chair, Yuan Chen, at 818-393-0940 or TP.Chair@iirw.org; the Vice Technical Program Chair, Lynett Westergard, at 208-234-6610 orTP.VChair@iirw.org; or the General Chair, John Conley, at 360-834-8668 or General.Chair@iirw.org. Web site: www.iirw.org.

REGISTER NOW!

Complete and send in the enclosed registration form. Please register early. We have sold out in past years. Space at the Camp limits IIRW to roughly 120 attendees.

We look forward to seeing you at the Workshop!

Sincerely,

Yuan Chen
Technical Program Chair

IIRW TRAVEL ARRANGEMENTS AND ACCOMMODATIONS

ARRIVAL AT CONFERENCE CENTER (a.k.a. CAMP)

Monday, October 16th: For those who are planning to attend the first tutorials, please plan to arrive *after* you have had your lunch. The Conference Center will **not** be prepared to serve you lunch. We will be ready to register you by 1:00 p.m. If you are coming later, we recommend you arrive before dark because the road from Route 89 is mostly one lane and winding.

TRANSPORTATION

The Stanford Sierra Conference Center is located at the far end of Fallen Leaf Lake, several miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Flight arrangements into Reno can be made through the *IEEE Travel Services*. Driving time from the Reno airport to the Stanford Sierra Conference Center is approximately two hours. Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the ***South Tahoe Express.*** With a scheduled request, Stanford Sierra Conference Center will provide transportation from the Casino to the Conference Center.

TRAVEL ARRANGEMENTS AND DISCOUNTS

Special discounted airfares for IIRW are available through IEEE Travel Services. Discounts are available with Continental Airlines. If you are flying on another carrier, contact IEEE Travel Services to check for other discounts by calling 1-800-879-4333 (US and Canada) and 1- 732-562-5387 (International) between the hours of 8:30 a.m. and 5:00 p.m. EST, Monday through Friday, or check http://www.ieeetravelonline.org and click on "Book a Flight." This secure site offers simple and convenient service through which you can search, reserve and ticket your travel anytime, anywhere. Discounts are only available through IEEE Travel Services for air.

Special car rental rates are available with the following companies:

National Car Rental	Discount Code: 5282921
Avis Rental Car	Discount Code: A606098
Budget Rental	Discount Code: X520000
Hertz Rental	Corporate Code: 61368, Permission Code: 937661
Enterprise Rental	Corporate CDP# NA24IE1

You may also fax or email your travel requirements including your travel dates, preferred departure and return times, and phone and fax numbers to the IEEE Travel Services; and a Travel Counselor will contact you promptly. Fax: +1 732 562 8815 ; e-mail address: travel-team@ieee.org

IEEE Travel goes the extra miles for its customers - more than today's no-service internet travel sites. Customers receive extra benefits like: dedicated, experienced travel counselors, 24-hour emergency service, automated fare quotes, and much more!

TRAVEL between RENO and SOUTH LAKE TAHOE

The South Tahoe Express **runs a shuttle from Reno to South Lake Tahoe** with departures from Reno on the hour from 10:00 a.m, to 7:00 p.m. and and the travel time is approximately 1½ hours. The shuttle costs $21 each way ($38 round trip) tickets can be purchased at the South Tahoe Express counter located in the baggage area in the Reno airport. Check http://www.southtahoeexpress.com/ to access the self serve ticketing system and verify schedules that are seasonal and subject to change or call 866-89-TAHOE or +1775 325-8944). Fuel surcharges (~$3.50 r.t.) are possible. The South Tahoe Express shuttle **leaves the Horizon Casino at South Lake Tahoe and returns to Reno** on the following schedule: 3:07 a.m., 5:07, 7:37, 8:37, 10:37, 12:37, 1:37 p.m., 2:37, 3:37, 5:37, and 8:52 p.m. Tickets may be purchased at the main cashier's cage in the Horizon Casino.

TRAVEL between SOUTH LAKE TAHOE and STANFORD SIERRA CONFERENCE CENTER

Stanford Sierra Conference Center offers courtesy transportation for conference attendees from the Horizon Casino between 12:30 p.m. and 11 p.m. on Registration Day (Monday, Oct. 16). Return trips to the Casino are offered on the last day of the conference only. If you are planning on using the South Tahoe Express, please notify Stanford Sierra Conference Center (530-541-1244) at least ONE WEEK prior to your arrival date. If you find yourself stranded, please call the Conference Center at the same number. The IRW Arrangements Committee may be able to provide emergency service to and from the casino. To schedule SSCC shuttle pickup service via the internet visit http://www.stanfordalumni.org/learningtravel/sierra/sierra-center/shuttle.html.

ACCOMMODATIONS

The Stanford Sierra Conference Center provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note that while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. Towels and soap are provided. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks. Please be aware of the following items:

- All participants must stay at the camp during the workshop.
- We cannot accommodate spouses or any companions at the camp.
- Accommodations are not available at the Stanford Conference Center for any day before or after the workshop.
- Smoking is permitted outdoors only. Smoking is not permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3968.
- A message board will be available for incoming calls: (530) 541-1244.
- There are pay telephones for outgoing calls and there are no telephones in the rooms.
- Please have lunch before you arrive at the Conference Center, there is no lunch available on Monday.

RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees. Enjoy IIRW!

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the Conference Center. A small flashlight would be helpful to find your cabin after dark.

See http://www.iirw.org/Directions_from_Reno_Airport.htm for detailed driving directions from the Reno Airport to Conference Center.