

2007 IEEE International Integrated Reliability Workshop

<http://www.iirw.org>

October 15-18, 2007

Stanford Sierra Conference Center, S. Lake Tahoe, CA



CALL FOR PAPERS

The Integrated Reliability Workshop focuses on ensuring semiconductor reliability through fabrication, design, testing, characterization, and simulation, as well as identification of the defects and physical mechanisms responsible for reliability problems. Through tutorials, discussion groups, special interest groups, and the informal format of the technical program, a unique environment is provided for understanding and developing reliability technology and test methodology for present and future semiconductor applications as well as for ample opportunities for discussions and interactions with colleagues.

Hot reliability topics for the workshop include: high-k and nitrided SiO₂ gate dielectrics, NBTI, Cu and other interconnects and low-k dielectrics, product reliability and burn-in strategy, impact of transistor degradation on circuit reliability, reliability modeling and simulation, SiGe and strained Si, III-V, SOI, optoelectronics, single event upsets, and reliability assessment of novel devices, future “nano”-technologies and emerging memory technologies.

We invite you to submit a presentation proposal that addresses any integrated semiconductor related reliability issue, including the following topics:

- **Designing-in reliability (products, circuits, systems, processes):**

methodologies and concepts, modeling and simulation tools, reliability-driven design rules and checkers, use of WLR and/or reliability test structures and methods for design rule verification, in-line detection and reliability analysis.

- **Customer product reliability requirements / manufacturer reliability tasks:**

limits to achieving future reliability targets, reliability evaluation methodologies and reporting systems, data bases, chip reliability, product reliability extrapolation to use conditions, wafer and package burn-in, packaging, strategies to eliminate burn-in, correlation between process, yield, and reliability, qualification strategies.

- **Root cause defects, physical mechanisms, and simulations**

nature of defects, physical and electrical characterization of defects, defect generation models, process induced defects and degradation, modeling/simulation of reliability related circuit constraints, accelerated testing and lifetime extrapolation..

- **Identification and characterization of reliability effects:**

failure mechanisms in new materials and device structures, reliability aspects of: high-k gate stack, Cu and other interconnects and low-k dielectrics, MOS and bipolar transistors including FinFETs and 3D gates, SiGe and strained Si, SOI, MEMS devices, optoelectronics, high voltage devices, unique reliability phenomena and failure mechanisms in Non-Volatile memories, new memory technologies, MRAM, nanotechnology reliability assessment, and limits to accelerated stressing.

- **Deep sub-micron transistor and circuit reliability:**

single event effects and soft errors, ESD, electromigration, mechanical stress related issues, hot carrier effects, NBTI, dielectric breakdown, reliability extrapolation, impact of new material systems, modeling and simulation, impact of scaling,

- **Wafer level reliability tests, test approaches, and reliability test structures:**

fast stress tests and analysis methodologies, reduction in development time, in-line monitors, relation to circuit-element and package-level tests, use and interpretation of WLR data, success stories, fine tuning of WLR implementation, accounting for censoring, design, characterization, and data analysis for chip or package level circuit-like structures (including electrical and/or physical test/analysis).

PAPER AND POSTER SUBMISSION INSTRUCTIONS

Abstract Submission Deadline: *July 13, 2007*

Your *two page extended abstract* (maximum two pages including figures) should state clearly and concisely the results of your work and why they are significant. Representative data and figures that support your proposal are **REQUIRED**.

Please e-mail your abstract to the Technical Program Chair *either as an MS Word document or .pdf attachment*. Fax submissions of abstracts will **NOT** be accepted. A separate covering letter must include your full business address, i.e., author name, affiliation, address, telephone and fax numbers, and the e-mail address for each co-author. State whether *oral or poster*

presentation is preferred. All submissions will be acknowledged by email within three weeks. If you do not receive acknowledgment of your submission, please contact the Technical Program Chair.

Viewgraphs for all accepted oral presentations are required by September 8, 2007 for inclusion in the Presentation Handout that is distributed at the workshop. A written version of your presentation is due at the workshop for inclusion in the well known Final Report.

Expanded versions of selected workshop manuscripts will be published in an Integrated Reliability Workshop Special Proceedings Issue of IEEE Transactions in Device and Material Reliability (TDMR), June 2008.

Late paper Submission: A limited number of late breaking news full length manuscripts will be considered and may be submitted until September 7, 2007. Accepted late papers will be included in the Final Report.

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LODGING & FACILITIES

Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, a few miles from South Lake Tahoe, are clusters of 2 and 3 bedroom cabins furnished in the rustic style of an alpine resort. Each cabin is equipped with shared bathroom facilities. All rooms have decks with magnificent views of Fallen Leaf Lake and the surrounding Sierra peaks.

The physical isolation of the location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees.

Lodging can only be provided to registered attendees of IRW in accordance with housing rules.

SPONSORS

The International Integrated Reliability Workshop is sponsored by

the IEEE Electron Device Society

and



the IEEE Reliability Society

and



in doing so the IIRW is IEEE published and archived.



MORE INFORMATION

For more details and information, including pictures of the environment as well as topics presented at the workshop in previous years, please see our web-page:

<http://www.iirw.org>