



IEEE/Integrated Reliability Workshop
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PROGRAM ANNOUNCEMENT

You are cordially invited to participate in the 2007 Integrated Reliability Workshop. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. You will have the opportunity to closely interact with your peers in moderated discussion groups, open poster sessions, technical sessions, tutorials, and special interest groups. All Workshop activities take place in a relaxed and rustic setting that promotes interactive learning and discussion. You should come away from the workshop intellectually stimulated and refreshed.

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 Harry Schafft, NIST
 John F. Conley Jr., Sharp

MAJOR TECHNICAL THEMES

The Integrated Reliability Workshop covers a wide and well-balanced spectrum of pressing reliability challenges, preparing attendees for reliability problems at hand and those to come. The focus points reflected by this year's program include gate dielectric reliability, transistor reliability including NBTI and hot carrier aging, interconnect reliability covering metal line and via electromigration and stress migration, memory reliability, and product reliability.

This year's workshop features six tutorials by world leading experts. Topics include current issues SRAM reliability, reliability issues in floating gate flash memories, reliability methodology for high-k gate stacks, detection of atomic scale defects involved in MOS reliability problems, and device scaling and reliability for outer space applications. The tutorials will be on Monday and Tuesday afternoon.

Our keynote on Tuesday morning will be given by Sammy Kayali of the Jet Propulsion Laboratory, California Institute of Technology on "Microelectronics for Space Applications - Challenges and Opportunities."

As usual, all authors, including the tutorial speakers and the keynote speaker will be available for discussions during the workshop. Ample time is scheduled for one-on-one exchanges, organized discussion groups, the popular and productive SIGs (Special Interest Groups), inter-session breaks, and poster sessions where all attendees are encouraged to display a poster and discuss their most recent work, ideas, and results. Wednesday afternoon is available for recreation with fellow attendees, a great way to become more acquainted with your colleagues.

Overall this represents an exciting, well-balanced program that addresses the needs and interests of today's reliability engineers for the benefit of their company. We invite you to tell your colleagues and your managers about this year's IIRW. Make a point to let them know that both the attendees and their organizations gain from this investment in learning, which helps in dealing with today's challenges and preparing for tomorrow's.

'07 Workshop Features:

- ★ **Keynote: Microelectronics for Space Applications - Challenges and Opportunities—Sammy Kayali, Jet Propulsion Laboratory, California Institute of Technology**
- ★ **Group Discussions**
 - High-k Reliability
 - NBTI
 - Interconnect Reliability
 - Product/Circuit Reliability
- ★ **6 Tutorials**
 - Detection of Atomic Scale Defects in MOS Reliability Problems
 - Current Issues in SRAM Reliability
 - Reliability of Floating-Gate Flash Memories
 - Reliability Assessment Methodology for High-k Gate Stacks
 - Beam-Based Defect Localization in ICs
 - Semiconductor Device Scaling: General Trends and Reliability Implications for Space
- ★ **20 Technical Presentations on:**
 - Interconnect Reliability
 - Ultra-Thin Oxides / High-k Reliability
 - NBTI/Hot Carrier Aging
 - Capacitor and Resistor Reliability for Mixed Signal
 - Memory Reliability
 - Product Reliability
 - Wafer Level Reliability
- ★ **10 Refereed Posters + Open Poster Sessions**
- ★ **Special Interest Groups**



KEYNOTE

MICROELECTRONICS FOR SPACE APPLICATIONS - CHALLENGES AND OPPORTUNITIES

*Sammy Kayali, Jet Propulsion Laboratory,
California Institute of Technology*

New space system implementations require the use of advanced microelectronic devices in critical applications. System demands such as increases in functionality and reduction of mass, power and volume make the need for such advanced microelectronic devices more pressing. However, newly developed advanced microelectronic devices lack the traditional reliability and characterization data necessary for qualification for insertion into space systems.

The growth and maturity of the semiconductor industry has resulted in substantial improvements in processing methods, fabrication yield, and overall quality of commercially viable semiconductor devices. This coupled with large volume production and the utilization of statistical process control has greatly reduced the infant mortality population across the industry. However, reproducibility of a product does not guarantee reliability in the intended application. For critical space applications where the success or failure of a mission hinges on the lifetime and performance of a single device; it is critical that all aspects of the reliability and the various known failure modes and mechanisms be addressed prior to the insertion of the component in the application.

The selection and application of microelectronic components in high reliability space systems requires knowledge of the component design, fabrication process, and applicable tests. In addition, reliability analysis and detailed knowledge of the application environment is necessary in order to determine the suitability of the selected component for the application. These issues are of particular importance for the application of semiconductor devices in high reliability systems due to the need for the utilization of large numbers of these devices at the upper limit of their performance and stress capabilities.

In order to collect the reliability and characterization data required for space qualification, an in-depth understanding of the material characteristics, fabrication processes, and relevant failure mechanisms of the technology is necessary. This presentation will provide a description of some of the technical and programmatic challenges affecting the insertion of advanced microelectronics in NASA/JPL flight applications and the methodology necessary to ensure the desired reliability.

TUTORIALS

Chair: Bill Tonti

Co-Chair: Tomasz Brozek

BEAM-BASED DEFECT LOCALIZATION IN ICs

Edward I. Cole Jr., Sandia National Laboratories

Tutorial A1, Monday, 1:30-3:30 p.m. (Angora Room)

This tutorial will review standard and new electron and laser based tools for localizing defects, including so-called "soft" defects and what's being done in solid immersion lens technology for improving backside spatial resolution, with a few comments on the future. Best practices and limitations will also be discussed. All of these techniques can be performed on a standard SEM or SOM (using the proper laser wavelengths). The tutorial's goal is to provide beneficial information to both novice and experienced failure analysts. Topics are: 1) Standard techniques: secondary electron imaging for surface topology, voltage contrast, capacitive coupling voltage contrast, backscattered electron imaging, and electron beam induced current imaging; 2) Specialized SEM techniques: novel voltage contrast applications, resistive contrast imaging, and charge-induced voltage alteration (both high and low energy versions); and 3) SOM techniques: light-induced voltage alteration, thermally-induced voltage alteration/optical beam induced resistance change, Seebeck Effect imaging, soft defect localization, and light alteration defect analysis.

SEMICONDUCTOR DEVICE SCALING:

GENERAL TRENDS AND RELIABILITY IMPLICATIONS FOR SPACE

Allan Johnston, JPL

Tutorial A2, Monday, 1:30-3:30 p.m. (Cathedral Room)

Advanced semiconductor devices continue to advance at an almost unprecedented rate, requiring extensive changes in the underlying device structure. This paper will discuss general features of device scaling, discussing some of the tradeoffs that affect reliability. Additional de-rating factors are usually required to use these devices in space, as well as system-level designs that incorporate fault tolerance. Space radiation imposes additional difficulties, including catastrophic latchup from energetic cosmic rays. In some cases scaling helps radiation hardness, but it can also make radiation problems more severe. The material will be based on recent advances in the reliability and radiation effects literature, as well as on specific experience at JPL in qualifying and fielding space systems. A brief discussion of radiation hardened methods will also be included.

Several topics will be included, including

- Reliability and scaling issues for rad-hard devices
- Reliability of SOI vs. bulk rad-hard, and
- Rad-hard circuit design

DETECTION OF ATOMIC SCALE DEFECTS IN MOS RELIABILITY PROBLEMS

Patrick Lenahan, Penn State

Tutorial B1, Monday, 4:00-6:00 p.m. (Angora Room)

This tutorial will have two goals. (1) This tutorial will introduce attendees to magnetic resonance techniques which have the power to identify the atomic-scale defects involved in MOS reliability problems. (2) This tutorial will provide a fairly detailed discussion of magnetic resonance results on reliability defects involved in several areas: negative bias temperature stressing of SiO₂ and plasma-nitrided oxide pMOSFETs, interface/interlayer dielectric/bulk trapping centers in HfO₂-based MOS devices, hot carrier induced defects, and stress induced leakage defects which may be important for flash memory reliability. An attempt will be made to integrate the two aspects of the presentation by illustrating particular resonance techniques with application to specific reliability issues. For example, the electrically detected magnetic resonance techniques of spin-dependent tunneling and spin-dependent recombination are very useful in studies of the negative bias temperature instability. These techniques will be discussed, in part, in the context of NBTI related measurements. Conventional electron spin resonance has been quite useful in studies of trapping defects in HfO₂ and SILC related defects in conventional oxides. HfO₂ trapping and SILC defects will be utilized as specific examples in a discussion of conventional electron spin resonance.

CURRENT ISSUES IN SRAM RELIABILITY

Bruce Woolery, Intel

Tutorial B2, Monday, 4:00-6:00 p.m. (Cathedral Room)

The drive for increased functionality and performance of integrated circuits drives greater integration, including the integration of larger embedded memories. The technology enablers for larger memories include smaller dimensions, new materials, and new device structures, each with reliability risks. In this tutorial, we will discuss the impacts of leakage and Vt shifts, device scaling impact, narrowing Vdd window, and the advantage of error correction.

RELIABILITY OF FLOATING-GATE FLASH MEMORIES

Neal Mielke, Intel

Tutorial C1, Tuesday, 3:00-5:00 p.m. (Angora Room)

This tutorial reviews the basic operation of NOR and NAND floating-gate Flash memories and then describes their dominant reliability degradation mechanisms. Media-management methods in component and system design for dealing with these mechanisms are covered. Finally, product and technology qualification methods are discussed.

(continued on back of registration form)

MONDAY, October 15 Please have lunch before arriving at the camp; no lunch will be served at the camp.

- 1:00–6:00 p.m. Registration: Pick up badges & handout (*Lodge Lounge*)
Discussion Group and SIG Signup; Poster preparation
- 1:00–8:00 p.m. Lodge check-in. Get room assignment (prearranged) & room key.
(If physically challenged please notify desk of special needs.)
- 1:30–6:00 p.m. **Tutorials** (Parallel Sessions A & B): Chair: Bill Tonti, IBM and Tomasz Brozek, PDF Solutions

| Tutorials | Parallel Session | Angora Room | Cathedral Room |
|-----------|----------------------------|----------------------|----------------|
| 1:30–3:30 | A | A1: Failure Analysis | A2: Radiation |
| 3:30–4:00 | Break (poster preparation) | | |
| 4:00–6:00 | B | B1: ESR | B2: SRAM |

- 6:15–7:30 p.m. DINNER, (*Dining Room*) authors: dine with your session chair
- 7:30–10:30 p.m. Announcements and Poster Session & Mixer (*Cathedral Room*)
Poster Session Chair: Guoqiao Tao, NXP Semiconductor

TUESDAY, October 16

- 7:00–8:00 a.m. BREAKFAST (*Dining Room*)
- 8:00–8:15 a.m. Welcome & Introduction: Yuan Chen, General Chair
Technical Program Overview: Pat Lenahan, Technical Program Chair
- 8:15–9:15 a.m. **Keynote:** Microelectronics for Space Applications—Challenges and Opportunities—Sammy Kayali, Jet Propulsion Laboratory, California Institute of Technology
- 9:15–9:25 a.m. Break
- 9:25–11:30 a.m. **Session #1: NBTI**, Chairs: Bill Knowlton, Boise State University, and Chad Young, SEMATECH
- 1.1 A new smart Vth-extraction methodology considering recovery and mobility degradation due to NBTI—C. Schlünder, M. Hoffmann, R.-P. Vollertsen, G. Schindler, W. Heinrigs, W. Gustin, and H. Reisinger, Infineon
 - 1.2 A rigorous study of measurement techniques for negative bias temperature instability—Tibor Grasser, Paul-Jurgen Wagner, Philipp Hehenberger, Wolfgang Gös, TU Wien; Ben Kaczer, IMEC
 - 1.3 Atomic-scale defects involved in NBTI in plasma-nitrided pMOSFETs—J.P. Campbell, P.M. Lenahan Penn State University; A.T. Krishnan, S. Krishnan, Texas Instruments
 - 1.4 Effect of NBTI degradation on transistor variability in advanced technologies—Sangwoo Pae, Jose Maiz, Chetan Prasad, Intel
 - 1.5 Enhanced PMOS NBTI degradation due to halo implant channeling in a DGO CMOS process—D. Brisbin, J. Yang, S. Bahl, C. Parker, NSC
- 11:30–12:00 p.m. Group Picture
- 12:00–1:00 p.m. LUNCH, *Dining Room*
- 1:15–2:30 p.m. **Session #2: NBTI and Related Topics**, Chair: Tibor Grasser, TU Wien
- 2.1 Charging and discharging of oxide defects in reliability issues—Wolfgang Gös, Tibor Grasser, TU Wien
 - 2.2 SRAM stability analysis considering gate oxide SBD, NBTI and HCI—Jin Qin, University of Maryland; Xiaojun Li, Intel; Joseph B. Bernstein, University of Maryland;
 - 2.3 Investigation of NBTI recovery induced by conventional measurements for pMOSFETs with ultra-thin SiON gate dielectrics—Lei Jin, Mingzhen Xu, Peking University
- 2:30–3:00 p.m. Break
- 3:00–5:00 p.m. **Tutorials** (Parallel Session C): Chair: Bill Tonti, IBM and Tomasz Brozek, PDF Solutions

| Tutorials | Parallel Sess. | Angora Room | Cathedral Room |
|-----------|----------------|--|--|
| 3:00–5:00 | C | C1: Reliability of floating-gate flash memories | C2: Reliability assessment methodology for high-k gate stacks |

- 6:00–7:30 p.m. DINNER *Dining Room*
- 7:30–8:30 p.m. Poster Session and Mixer: Chair: Guoqiao Tao, NXP Semiconductor
- 8:30–9:30 p.m. **Discussion Groups:** Chair: Rolf Geilenkeuser, AMD
(One hour parallel sessions for each topic) Attendees are to participate in one of the groups
- 9:30–10:30 p.m. Individual SIG Meetings (to be announced at camp)

WEDNESDAY, October 17

- 7:00–8:00 a.m. BREAKFAST (*Dinning Room*)
- 8:00–8:15 a.m. Announcements, (*Angora Room*)
- 8:15–9:30 a.m. **Session #3: Memory Reliability**, Chair: Bill Tonti, IBM
- 3.1 Charge-gain program disturb mechanism in split-gate flash memory cell—Viktor Markov, Konstantin Korablev, Alexander Kotov, Yuri Tkachev, Xian Liu, James Yingbo Jia, Tho Ngoc Dang, and Amitay Levi, Silicon Storage Technology
 - 3.2 Scaling tunneling oxide to 50Å in floating-gate logic NVM at 65nm and beyond—Bin Wang, Martin Niset, Yanjun Ma, Hoc Nguyen and Ron Paulsen, Impinj
 - 3.3 A simple and accurate method to extract neutral threshold voltage of fresh and stressed floating gate flash devices—Guoqiao Tao, Helene Chauveau, Dick Boter, Do Dormans, and Rob Verhaar, NXP Semiconductors
- 9:30–10:00 a.m. Break
- 10:00–11:15 a.m. **Session #4: Transistor Reliability**, Chair: Andreas Martin, Infineon
- 4.1 New approach for the assessment of the effect of plasma induced damage on MOS devices and subsequent design manual rules—Andreas Martin, Infineon

- 4.2 Charge pumping revisited – the benefits of an optimized constant base level charge pumping technique for MOS-FET analysis—T. Aichinger, Kompetenzzentrum für Automobil und Industrie-Elektronik and M. Nelhiebel, Infineon Austria
- 4.3 Characterization and analysis of gate-induced-drain-leakage current in 45nm CMOS technology—Xiaobin Yuan, Jae-Eun Park, Jing Wang, Enhai Zhao, David Ahlgren, Terence Hook, Jun Yuan, Victor Chan, Huiling Shang, IBM; Chu-Hsin Liang, Richard Lindsay, Infineon; Sungjoon Park, Hyotae Choo, Samsung
- 11:15–12:05 p.m. **Session #5: Electromigration**, Chair: TBD
- 5.1 Electromigration multistress pattern technique for copper drift velocity and Black's parameter n extraction—L. Doyen, NXP; X. Federspiel, Qimonda; L. Arnaud, CEA LETI; F. Terrier, ST Microelectronics; Y. Wouters, SIMAP; V. Girault, ST Microelectronics
- 5.2 Optimized structure design for wafer level electromigration test—X. Federspiel, Qimonda; D. Ney, ST Microelectronics; L. Doyen, NXP and G. Sers, Qimonda
- 12:05–1:30 p.m. LUNCH (*Dining Room* — Take out Lunch bags available)
- 1:30–6:00 p.m. Open The afternoon is free for discussion, hiking & other recreation
- 6:00–7:30 p.m. DINNER, *Dining Room*
- 7:30–8:30 p.m. Mixer & Poster Session: Guoqiao Tao
- 8:30–9:30 p.m. **Discussion Groups**: Chair: Rolf Geilenkeuser, AMD
- 9:30–10:30 p.m. **Individual SIG Meetings** (to be announced at camp)

THURSDAY, October 18

- 7:00–8:00 a.m. BREAKFAST (*Dining Room*)
- 8:00–8:10 a.m. Announcements, (*Angora Room*)
- 8:10–9:00 a.m. **Session #6: Fuse Reliability**, Chair: Guoqiao Tao, NXP Semiconductor
- 6.1 Programming conditions for silicided poly-Si or copper electrically programmable fuses—Hiroyuki Suto, Shigetaka Mori, Michihiro Kanno, and Naoki Nagashima, Sony
- 6.2 Reliability investigation of NIPTSI electrical fuse with different programming mechanism—C. Tian, D. Moy, B. Messenger, C. Kothandaraman, J. Safran, S. Wu, P. Wang, N. Robson and SS. Iyer, IBM
- 9:00–9:50 a.m. **Session #7: High-K Reliability**, Chair: Gennadi Bersuker, SEMATECH
- 7.1 Defects in the interfacial layer of SiO₂-HfO₂ gate stacks: Depth distribution and identification—O. Ghobar, D. Bauza, IMEP, MINATEC; B. Guillaumot, CEA LETI, ST Microelectronics
- 7.2 Charge trapping and dielectric relaxation of tri-layer ZrHfO_x/RuO_x/ZrHfO_x high-k thin films—Rui Wan, University of Tennessee; Chen-Han Lin, Yue Kuo Texas A&M University; and Way Kuo, University of Tennessee
- 9:50–10:15 a.m. Break (Time to check out!)
- 10:15–11:15 a.m. **Session #8: Late News, Chair**, Jason Campbell, NIST
- 8.1 Positive charge generation by PBTI stress in nMOS high-k devices—D. Heh, P.D. Kirsch, C.D. Young, G. Bersuker, SEMATECH
- 8.2 Direct observation of electrically active interfacial layer defects which may cause threshold voltage instabilities in HfO₂ based MOSFETs—J.T. Ryan and P.M. Lenahan, Penn State University
- 8.3 Characterization of interface and bulk oxide traps in SiC MOSFETs with epitaxially grown and implanted channels—M. Gurfinkel et al., Tel Aviv Univ., Univ. of Maryland, NIST
- 11:15–12:15 p.m. **DG Summary / SIG Report / Wrap-up**
- 12:15–1:25 p.m. LUNCH, (*Dining Room*) & then the Workshop Ends— Attendees must Leave the Stanford Sierra Camp unless attending JC14.2

2:00 p.m. Thursday to noon Friday JEDEC 14.2 Committee on Wafer Level and Technology Reliability

2007 IIRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 18-19)

Meeting registration automatically includes a room reservation.

(Please type, print or attach business card)

NAME: _____
Last First Initial

COMPANY: _____
Mail Stop

ADDRESS: _____
City State/Country Zip/Postal Code

Phone: (_____) _____ Fax: _____

Email: _____

For cabin assignments: male female

Address is HOME

Please check here if you do not wish to receive mail other than from IIRW & IRPS

Please check here if physically challenged and you require any auxiliary aids or services.
 Please call (315) 339-3968.

Will bring poster. Title: _____

I am interested in the following Discussion Group(s):

Gate Oxide/High-k; NBTI; Interconnects; Product Reliability;

My Suggestion _____

Method of Payment: Check: Make checks payable to: **2007 IEEE/IIRW**

No wire transfers Credit Card: AMEX MASTER CARD VISA Diners Club

Card No. _____ Expiration Date _____ Signature _____

REGISTRATION FEES

IEEE Member (incl. mem# _____) **\$1200*** _____

NON-IEEE Member **\$1300*** _____

IEEE STUDENT** (mem# _____) **\$880*** _____

After 5-Oct-07 add late fee \$100 _____

* Includes workshop attendance & handout materials, tutorial attendance, 3 nights lodging (Monday—Wednesday) 9 meals (dinner Monday— lunch Thursday), Final Workshop Report with CD.

To promote student involvement at IIRW, we will be offering a reduced registration fee of \$880 to the **first 15 students who register. Students accepting the discount must be either IEEE member, or join the IEEE as a student member.

EXTRA COPIES of Workshop?

Final Report (printed) Qty: ___ x **\$80** _____

Final Report (CD) Qty: ___ x **\$80** _____

Final Report (printed & CD) Qty: ___ x **\$130** _____

JC-14.2 Mtg. accommodations*** **\$270** _____

*** Includes 1 night lodging (Thursday), 3 meals (dinner Thursday— lunch Friday)

TOTAL REMITTED \$ _____

No wire transfers Cancellation fees: \$50 after Sept. 21 ; full fee after Oct. 5

Send this completed form and payment to: IIRW Registration; P.O. Box 308; Westmoreland, NY 13490 Paying by credit card... fax to 315-336-9134
 Questions? becky@sar101.com or 315-339-3968 or web site: <http://www.iirw.org>

Gennadi Bersuker, SEMATECH

Tutorial C2, Tuesday, 3:00-5:00 p.m. (Cathedral Room)

High-k/metal gate stacks are entering the production stage that requires addressing practical characterization issues. It raises the question of how much we can rely on the extensive methodology/characterization experience accumulated for the conventional SiO₂-type dielectrics taking into account that the SiO₂ layer is usually a component of the multilayer high-k gate stack. The tutorial discusses general validity of the accelerated stress approach, and concentrates on delineating contribution to device instability from the high-k and oxide layers in order to assess stress-generated damage vs. activation of the process-related defects, which is critical for correct lifetime evaluation.

DISCUSSION GROUPS

Chair: Rolf Geilenkeuser, AMD

The evening discussion group program is a favorite highlight of the workshop experience. Attendees will have a choice of two areas on Tuesday and Wednesday evenings. The topics to be discussed will be at the discretion of those participating in the group. Each group is assigned a pair of leaders who have extensive experience with the area and will help to guide the discussion. Everyone is encouraged to bring along data and/or ideas to share on topics that are of particular interest. As we get closer to the date of the workshop, we will be surveying registered attendees so that we may prepare relevant discussion outlines to be distributed at the camp. This year's discussion areas and leaders are:

1. HIGH-K DIELECTRICS,
Chad Young, SEMATECH and Patrick Lenahan, Penn State
2. NBTI: Gennadi Bersuker, SEMATECH and Amr Haggag, Freescale
3. INTERCONNECTS: Jens Ullmann, Qualitau
4. PRODUCT/CIRCUIT RELIABILITY:
Andrew Turner, IBM and Bin Wang, Impinj

SPECIAL INTEREST GROUPS

Chair: Rolf Geilenkeuser, AMD

A Special Interest Groups (SIGs) is a collaborative working team focused on one compelling topic of mutual interest. The SIG program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. For more information on SIGs, please see <http://www.iirw.org/07/07SIG.html>.

REFEREED & OPEN POSTER SESSIONS

(Monday, Tuesday, and Wednesday Evenings)

Chair: Guoqiao Tao, NXP Semiconductor

In addition to our refereed poster sessions featured below, all attendees have the opportunity to present a poster to communicate and discuss their ideas and newest results on technical projects or issues. Please indicate in the space provided on the registration form your intention to bring a poster. A poster display board (32" x 40" or 81 cm x 100 cm) will be reserved for you. Your work should be in landscape format on 8½ x 11" or A4 paper with a maximum of twelve pages. This is a great opportunity for you to share your work with your peers. Also feel free to bring last minute results, board space will be found for you.

IIRW 2007 Refereed Posters:

- P1 Substrate injection disturb in high density flash FPGA devices, S.R. Kim, N. Chan, Actel, B. Sharokhi, University of Toronto, H. Micael, J. Yaonan, S. Samiee, K.J. Han, B. Cronquist, Actel
- P2 Fast wafer level reliability assessment of ultra thick oxides under impact ionization conditions, A. Aal, GOI Reliability
- P3 Observation of channel width independent HCI effect in 130nm technology, Santanu Mahapatra, Indian Institute of Science, Manjularani Kandachar, Santanu Samanta, Ramamohana Reddy, Avadh Kumar Tibrawal, Nitish Mathur, Helmut Puchner, Cypress Semiconductor
- P4 80V HVTMOS reliability characterization for 0.6um and 0.35um technologies, Colm Heffernan, Analog Devices
- P5 Comparison of line stress predictions with measured electromigration failure times, Rao R. Morusupalli, William D. Nix, Jamshed R. Patel, Stanford
- P6 Comprehensive hot carrier mechanism investigation of 40V LDNMOS transistor, Yi-Pin Chen, Yi-Chun Wang, Jih-San Li and Kuan-Cheng Su, UMC
- P7 Optimized reliability guardbands using variation aware junction temperature models, Paul Pereira, Daniel Kim, Peter O'Shea, PMC - Sierra
- P8 Process variabilities and performances in a 90nm embedded SRAM design, Michael Yap San Min, Philippe Maurine, LIRMM, Magali Bastian, Infineon, Michel Robert, LIRMM
- P9 Lead free discoloration due to tin oxidation – characterization, quality and reliability analysis, Rhea Manay, Intel
- P10 A reliability study in p-channel punchthrough for ASIC CMOS I/O buffer leakage, Erick Spory, ATMEL


JEDEC 14.2 MEETING. The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is \$270, which includes Thursday night dinner and lodging, and Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558, see www.jedec.org, or contact Al Strong (astrong@us.ibm.com), JC-14.2 Chair, at (802) 769-1326.

More Information. We expect an exciting workshop again this year. Your active participation in the many workshop activities and your active contributions to the technical discussions are key ingredients for the success of the workshop for all attendees. If you have additional questions, please contact either: me, the Technical Program Chair, Pat Lenahan, at 814-863-4630 or pmlsm@engr.psu.edu, or the Vice Technical Program Chair, Guoqiao Tao at Guoqiao.tao@NXP.com, or the General Chair, Yuan Chen, at 818-393-0940 or yuan.chen@jpl.nasa.gov. Web site: www.iirw.org.

REGISTER NOW!

Complete and send in the enclosed registration form. Please register early. We have sold out in past years. Space at the Camp limits IRW to roughly 120 attendees.

We look forward to seeing you at the Workshop!

Sincerely,

Pat Lenahan
Technical Program Chair

IIRW TRAVEL ARRANGEMENTS AND ACCOMMODATIONS

ARRIVAL AT CONFERENCE CENTER (a.k.a. CAMP)

Monday, October 15th: For those who are planning to attend the first tutorials, please plan to arrive *after* you have had your lunch. The Conference Center will **not** be prepared to serve you lunch. We will be ready to register you by 1:00 p.m. If you are coming later, we recommend you arrive before dark because the road from Route 89 is mostly one lane and winding.

TRANSPORTATION

The Stanford Sierra Conference Center is located at the far end of Fallen Leaf Lake, several miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Flight arrangements into Reno can be made through the *IEEE Travel Services*. Driving time from the Reno airport to the Stanford Sierra Conference Center is approximately two hours. Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the **South Tahoe Express**. With a scheduled request, Stanford Sierra Conference Center will provide transportation from the Casino to the Conference Center.

TRAVEL ARRANGEMENTS AND DISCOUNTS

Special discounted airfares for IIRW are available through IEEE Travel Services. Discounts are available with Continental Airlines. If you are flying on another carrier, contact IEEE Travel Services to check for other discounts by calling 1-800-879-4333 (US and Canada) and 1-732-562-5387 (International) between the hours of 8:30 a.m. and 5:00 p.m. EST, Monday through Friday, or check <http://www.ieeetravelonline.org> and click on "Book a Flight." This secure site offers simple and convenient service through which you can search, reserve and ticket your travel anytime, anywhere. Discounts are only available through IEEE Travel Services for air.

Special car rental rates are available with the following companies:

National Car Rental Discount Code: 5282921
Avis Rental Car Discount Code: A606098
Budget Rental Discount Code: X520000
Hertz Rental Corporate Code: 61368,
Permission Code: 937661
Enterprise Rental Corporate CDP#NA24IE1

You may also fax or email your travel requirements including your travel dates, preferred departure and return times, and phone and fax numbers to the IEEE Travel Services; and a Travel Counselor will contact you promptly. Fax: +1 732 562 8815 ; e-mail address: travel-team@ieeet.org

IEEE Travel goes the extra miles for its customers - more than today's no-service internet travel sites. Customers receive extra benefits like: dedicated, experienced travel counselors, 24-hour emergency service, automated fare quotes, and much more!

TRAVEL between RENO and SOUTH LAKE TAHOE

The South Tahoe Express runs a shuttle from Reno to South Lake Tahoe with departures from Reno on the hour from 10:00 a.m. to 7:00 p.m. and the travel time is approximately 1½ hours. The shuttle costs \$24 each way (\$43 round trip) tickets can be purchased at the South Tahoe Express counter located in the baggage area in the Reno airport. Check <http://www.southtahoexpress.com/> to access the self serve ticketing system and verify schedules that are seasonal and subject to change or call 866-89-TAHOE or +1775 325-8944). The South Tahoe Express shuttle leaves the Horizon Casino at South Lake Tahoe and returns to Reno on the following schedule: 3:37 a.m., 5:07, 7:37, 8:37, 10:37, 12:37, 1:37 p.m., 2:37, 3:37, 5:37, and 8:52 p.m. Tickets may be purchased at the main cashier's cage in the Horizon Casino.

TRAVEL between SOUTH LAKE TAHOE and STANFORD SIERRA CONFERENCE CENTER (SSCC)

You must schedule this final leg of the shuttle to the conference center at least one week before your arrival. SSCC offers courtesy transportation for conference attendees from the Horizon Casino between 12:30 p.m. and 11 p.m. on Registration Day (Monday, Oct. 15). Return trips to the Casino are offered on the last day of the conference only. **Notify SSCC (530-541-1244 or via internet) at least a week prior to your arrival date.** If you find yourself stranded, please call the Conference Center at the same number. The IIRW Arrangements Committee may be able to provide emergency service to and from the casino. To make advance arrangements for SSCC pickup via internet: <http://www.stanfordsierra.com/sitepages/pid57.php>

ACCOMMODATIONS

The Stanford Sierra Conference Center provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note that while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. Towels and soap are provided. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks. Please be aware of the following items:

- All participants must stay at the camp during the workshop.
- We cannot accommodate spouses or any companions at the camp.
- Accommodations are not available at the Stanford Conference Center for any day before or after the workshop.
- Smoking is permitted outdoors only. Smoking is not permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3968.
- A message board will be available for incoming calls: (530) 541-1244.
- There are pay telephones for outgoing calls and there are no telephones in the rooms.
- Please have lunch before you arrive at the Conference Center, there is no lunch available on Monday.

RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees. Enjoy IIRW!

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the Conference Center. A small flashlight would be helpful to find your cabin after dark.

See http://www.iirw.org/Directions_from_Reno_Airport.htm for detailed driving directions from the Reno Airport to Conference Center.

