IEEE/Integrated Reliability Workshop
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Westmoreland, NY 13490-0308

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# PROGRAM ANNOUNCEMENT

*You are cordially invited to participate in the 2008 Integrated Reliability Workshop. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. You will have the opportunity to closely interact with your peers in moderated discussion groups, open poster sessions, technical sessions, tutorials, and special interest groups. All Workshop activities take place in a relaxed and rustic setting that promotes interactive learning and discussion. You should come away from the workshop intellectually stimulated and refreshed.*

## Major Technical Themes

The Integrated Reliability Workshop covers a wide and well-balanced spectrum of pressing reliability challenges, preparing attendees for reliability problems at hand and those to come. The focus points reflected by this year's program include transistor reliability focusing on NBTI, reliability of advanced gate dielectric with emphases on high-K gate stack and devices, back-end reliability covering metal line and via electromigration and stress migration and reliability of thick dielectrics, reliability of sensors/ MEMS/Memories, reliability of compound materials and devices, and fast wafer level reliability monitoring.

This year's workshop features six tutorials by world leading experts. Topics include reliability-robust system design in scaled CMOS, NBTI, WLR standards development, measurement issues for high k and NBTI, efuse reliability and "Future" devices reliability discusssion. The tutorials will be on Sunday evening and Monday.

Our keynote on Monday morning will be given by Subramanyan "Dakshi" Dakshinamoorthy, Vice President for Reliability and Quality Assurance, Freescale Semiconductor.

As usual, all authors, including the tutorial speakers will be available for discussions during the workshop. Ample time is scheduled for one-on-one exchanges, organized discussion groups, the popular and productive SIGs (Special Interest Groups), inter-session breaks, and poster sessions where all attendees are encouraged to display a poster and discuss their most recent work, ideas, and results. Wednesday afternoon is available for recreation with fellow attendees, a great way to become more acquainted with your colleagues.

## '08 Workshop Features:

- **Keynote:** ***Subramanyan "Dakshi" Dakshinamoorthy, Vice President for Reliability and Quality Assurance, Freescale Semiconductor***
- **Group Discussions**
  - **High-k Reliability**
  - **NBTI**
  - **Interconnect Reliability**
  - **Product/Circuit Reliability**
- **6 Tutorials**
  - **Circuit Failure Prediction for Robust System Design in Scaled CMOS**
  - **Measurement Issues for High-k Technology including NBTI**
  - **JEDEC Overview**
  - **Toward Understanding NBTI**
  - **eFuse Design and Reliability**
  - **Reliability of "Future" Devices**
- **24 Technical Presentations on:**
  - **NBTI**
  - **Back-end Reliability**
  - **Reliability of Sensors,MEMS & Memories**
  - **High-k Reliability**
  - **Reliability of Compound Materials and Devices**
  - **fast Wafer Level Reliability**
  - **Late news**
- **10 Refereed Posters + Open Poster Sessions**
- **Special Interest Groups**

Overall this represents an exciting, well-balanced program that addresses the needs and interests of today's reliability engineers for the benefit of their company. We invite you to tell your colleagues and your managers about this year's IIRW. Make a point to let them know that both the attendees and their organizations gain from this investment in learning, which helps in dealing with today's challenges and preparing for tomorrow's.

–over–

# KEYNOTE

### Zero Defects Quality and Reliability Challenges for Growing Markets

Subramanyan "Dakshi" Dakshinamoorthy,
Vice President for Reliability and Quality Assurance,
Freescale Semiconductor

Freescale Semiconductor anticipates future industry growth in consumer, automotive, industrial and networking markets. Smart semiconductors expect to become more pervasive in automotive markets as consumer demand reacts to rising energy costs. And the semiconductor presence within the medical market grows, in part due to the increasing amount of healthcare required by the Baby Boomer generation, and also by the elevation of the quality of care afforded through microelectronic devices. Given expected growth in the noted markets, there is a continuous push to deliver Zero Defects quality and reliability

Meeting these requirements becomes challenging as technology scales and wear-out mechanisms such as NBTI have a stronger impact. New DFT/DFM/containment methodologies as well as supporting data for delivering Zero Defects quality will be discussed in addition to new reliability methodologies and supporting data for guardbanding power (Vmin) and speed (Fmax) against wear-out mechanisms.

# TUTORIALS

*Chair: Drew Turner*

### Circuit Failure Prediction for Robust System Design in Scaled CMOS

*Subhasish Mitra, Stanford University*

Tutorial #1, Sunday, 7:30-9:00 p.m. (Angora Room)

Circuit failure prediction predicts the occurrence of a circuit failure “before” errors actually appear in system data and states. This is in contrast to classical error detection where a failure is detected after errors appear in system data and states. Circuit failure prediction is performed concurrently during system operation or during periodic on-line self-test by analyzing the data collected by special circuits called “sensors” inserted at strategic locations inside a chip. This talk demonstrates the concept of circuit failure prediction, practical implementation of the concept, and its effectiveness in overcoming major scaled-CMOS reliability challenges such as early-life failures (also called infant mortality) and aging. The concept of circuit failure prediction also provides insignts into early-life failure behaviors that may be used in developing new techniques for screening early-life failure candidates during production test.

### Measurement Issues for High-k Technology including NBTI

*Chadwin Young, SEMATECH*

Tutorial #2, Monday, 9:25-10:55 a.m. (Angora Room)

This tutorial will be comprised of several parts that address various measurement methodologies required for properly characterizing high-k gate stacks. While discussing these techniques, emphasis will be placed on proper instrumentation and set up, followed by proper data analysis and interpretation. Some of the key methodologies that will be discussed are: Capacitance – Voltage (C-V), Pulsed Current – Voltage (I-V), and reliability evaluation techniques. The intended outcome of this tutorial is for the attendees to leave with a better understanding of high-k characterization requirements that he/she can implement in everyday measurements and have increased insight about these novel gate stacks.

### JEDEC Overview

*Alvin Strong, IBM*

Tutorial #3, Monday, 10:55-11:45 a.m. (Angora Room)

JEDEC is the leading developer of standards for the solid-state industry. However for some, there may be a mist about JEDEC that clouds the what JEDEC really is and really does. The intent of this tutorial is to clarify everyone’s understanding of the mission of JEDEC, to show the breadth of JEDEC, and to give the opportunities of service. The focus will be on JEDEC 14.2 since this is the JEDEC committee that is responsible for Wafer Level Reliability. Furthermore that focus will be on our most recent standards and those currently on our agenda including the update to the Foundry Guidelines.

### Towards Understanding Negative Bias Temperature Instability

*Tibor Grasser, Technical University of Vienna*

Tutorial #4, Monday, 1:00-2:30 p.m. (Angora Room)

Modeling efforts of negative bias temperature instability date back to the work of Jeppson and Svensson in 1977, who proposed the basic form of the popular reaction-diffusion model. This model is still at the heart of many modeling attempts today. However, recent research indicates that even refined variants of this model, while getting some features of NBTI right, cannot capture some crucial aspects of the phenomenon, most notably its ubiquitous logarithmically-decaying recovery phase. Consequently, alternative models have been developed. Some of these models, like the extensions based on dispersive transport of the released hydrogen species, predict like the underlying reaction-diffusion model, that the overall degradation is controlled by (dispersive) diffusion of hydrogen. Alternatively, some models assume that the actual depassivation reaction is the rate limiting step. On top of the creation of interface states, some authors have argued that trapped holes form a considerable part of the overall degradation. Despite all the efforts, however, no universally accepted theory of NBTI is available today, with published models covering only some aspects of the phenomenon and giving contradictory predictions of other aspects. This tutorial attempts to give a broad review of published modeling attempts, comparing their strengths and weaknesses, and eventually listing the requirements for a more complete model of NBTI.

### eFuse Design and Reliability

*William Tonti, IBM*

Tutorial #5, Monday, 2:50-4:20 p.m. (Angora Room)

Programmable eFuse designs present an integration challenge in modern CMOS processing. The power level to program a fuse, and the programming methodologies leverage reliability mechanisms which all other elements in a design avoid. A high degree of eFuse process control and circuit design is required in order to guarantee operation. Almost all eFuse types are one time programmable and are limited to “one chance” programmable. This paper will discuss selected eFuse technologies describing the design philosophy, electrical programming and characterization, the physics of failure, and some of the many applications an on chip programmable element provides.

### Reliability for "Future" Devices

*Wilfried Haensch, IBM TJ Watson Research Center*

Tutorial #6, Monday, 4:30-5:15 p.m. (Angora Room)

Device design has enjoyed over three decades of scaling leaving the fundamental device architecture basically unchanged. With $SiO_2$ gate dielectric hovering around 1 nm for the high performance space device engineers looked at different methods than scaling for performance boost. Stress enhancement of mobility is a prime example for a non scaling based performance booster. With the successful implementation of High-k dielectrics there is hope that the path to scaling is opened up again. In spite of the rapid advancement in gate dielectric scaling, most likely fully depleted devices will be needed to continue the density scaling of the past. We will discuss some of the challenges and opportunities that are related to the change of device architecture and requirements to continue the trend in integration density. The presentation will outline the path down to the ultimate FET device.

*(continued on back of registration form)*

# 2008 IEEE INTERNATIONAL INTEGRATED RELIABILITY WORKSHOP PROGRAM (preliminary)

IEEE — Electron Devices Society — Reliability Society

## SUNDAY, October 12 Please have lunch before arriving at the camp; no lunch will be served at the camp.

| | |
|---|---|
| 3:00–6:00 p.m. | Registration: Pick up badges & handout (*Lodge Lounge*)<br>Discussion Group and SIG Signup; Poster preparation |
| 3:00–8:00 p.m. | Lodge check-in. Get room assignment (prearranged) & room key.<br>(If physically challenged please notify desk of special needs.) |
| 6:15–7:30 p.m. | DINNER, *(Dining Room)* authors: dine with your session chair |
| 7:30–9:00 p.m. | **Tutorial #1: Circuit Failure Prediction for Robust System Design in Scaled CMOS**—Subhasish Mitra, Stanford University |

## MONDAY, October 13

| | |
|---|---|
| 7:00–8:00 a.m. | BREAKFAST *(Dining Room)* |
| 8:00–8:10 a.m. | (Angora Room) Welcome & Introduction: Pat Lenahan, General Chair |
| 8:10–9:00 a.m. | **Keynote:** Subramanyan "Dakshi" Dakshinamoorthy, Vice President for Reliability and Quality Assurance, Freescale Semiconductor |
| 9:00–9:10 a.m. | Technical Program Overview: Guoqiao Tao, Technical Program Chair |
| 9:10–9:25 a.m. | Break |
| 9:25–10:55 a.m. | **Tutorial #2: Measurement Issues for High-k Technology including NBTI**—Chadwin Young, SEMATECH |
| 10:55–11:45 a.m. | **Tutorial #3: JEDEC Overview**—Alvin Strong, IBM |
| 12:00–1:00 p.m. | LUNCH, *Dining Room* |
| 1:00–2:30 p.m. | **Tutorial #4: Torward Understanding Negative Bias Temperature Instability**—Tibor Grasser, Technical Univ. of Vienna |
| 2:30–2:50 p.m. | Break |
| 2:50–4:20 p.m. | **Tutorial #5: eFuse Design and Reliability**—William Tonti, IBM |
| 4:30–5:15 p.m. | **Tutorial #6: Reliability of "Future" Devices**—Wilfried Haensch, IBM |
| 6:00–7:30 p.m. | DINNER, *(Dining Room)* authors: dine with your session chair |
| 7:30–10:30 p.m. | **Announcements / Poster Session & Mixer** *(Cathedral Room)*<br>Poster Session Chair: Chadwin Young, SEMATECH |

## TUESDAY, October 14

| | |
|---|---|
| 7:00–8:00 a.m. | BREAKFAST *(Dining Room)* |
| 8:00–8:15 a.m. | Announcements (Angora Room) |
| 8:15–9:30 a.m. | **Session #1: NBTI-1**, Chair: Pat Lenahan, PSU<br>1.1 The effect of recovery on NBTI characterization of thick non-nitrided oxides—H. Reisinger, R.P. Vollertsen, P.J. Wagner *, S. Aresu, W. Gustin, T. Grasser *, and C. Schlünder, Infineon Technologies *TU Wien<br>1.2 Total recovery of defects generated by negative bias temperature instability—C. Benard* **, J.-L. Ogier*, and D. Goguenheim ***, STM*, CNRS**, ***ISEN-Toulon<br>1.3 Advanced On-The-Fly method with correction of initial values to characterize negative bias temperature instability reliability—C. Benard* **, J.-L. Ogier*, and D. Goguenheim ***, STM*, CNRS**, ***ISEN-Toulon |
| 9:30–10:00 a.m. | Break |
| 10:00–11:20 a.m. | **Late News Presentations,** Chair: Guoqiao Tao, NXP<br>LN1 Defect creation stimulated by thermally activated hole trapping as the driving force behind negative bias temperature instability in $SiO_2$, SiON, and high-k gate stacks—Tibor Grasser[*], Ben Kaczer[%], Thomas Aichinger[†], Wolfgang Gös[*], and Michael Nelhiebel[‡] [*]TU Wien; [%]IMEC; [†]KAI; [‡]Infineon Technologies<br>LN2 The effect of the subthreshold slope degradation on NBTI device characterization—D. Brisbin & P. Chaparala, National Semic.<br>LN3 Reliability guardband reduction by differential targeting of pMOS gate oxide thickness—R. Geilenkeuser, K. Wieczorek, M. Trentzsch, F. Graetsch, B. Bayha, V. Samohvalov, T. Paetzold, and T. Schink, AMD<br>LN4 The origins of random telegraph noise in highly scaled SiON nMOSFETs—J.P. Campbell[1], J. Qin[1,2], K.P. Cheung[1], L. Yu[1,3], J.S. Suehle[1], A. Oates[4], and K. Sheng[3] [1]NIST; [2]University of Maryland; [3]Rutgers University; [4]TSMC |
| 11:20–12:00 p.m. | Group Picture |
| 12:00–1:00 p.m. | LUNCH, *Dining Room* |
| 1:15–2:55 p.m. | **Session #2: Back-end Reliability,** Chair: Gaddi Haase, TI<br>2.1 Copper line topology impact on the reliability of SiOCH low-k dielectrics for the advanced 45nm technology node and beyond—M. Vilmay[(1)], D. Roy[(1)], C. Monget[(1)], F. Volpi[(2)], J-M. Chaix[(2)] [(1)]STM ; [(2)]SIMAP<br>2.2 Impact of oxygen vacancies profile and fringe effect on leakage current instability of tantalum pentoxide metal-insulator-metal (MIM) capacitors—Vi. Martinez, STM & IMEP/LAHC, C. Besset, F. Monsieur, STM, L. Montès, and G. Ghibaudo, IMEP-LAHC<br>2.3 The influence of complex geometries and stress non-uniformity on reliability—A. Aal, ELMOS Semiconductor AG<br>2.4 Stress characterization for stress-induced voiding in Cu/Low K interconnects with geometry and upper cap layer dependences—M. Lin, J.W. Liang, and K.C. Su, UMC |
| 2:55–3:15 p.m. | Break |
| 3:15–5:30 p.m. | **Session #3: Reliability of Sensors/MEMS/Memories,** Chair: William Tonti, IBM<br>3.1 Ageing under illumination of MOS transistors for active pixel sensors (APS) applications—D. Lopez * **, F. Monsieur * and F. Balestra **, *STM, ** IMEP-LAHC<br>3.2 Creep behavior of PZT actuated micro-optical modulator—H.Y. Kim, E.M. Bourim, J.S. Yang, J.H. Yang, K.S. Woo, J.H. Song, and S.K. Yun, Samsung Electromechanics Co.<br>3.3 Investigation of GIDL current Injection disturb mechanism in two-transistor-eNVM memory devices—S.R. Kim, K.J. Han, J. Lee*, P.Y. Lee, T. Zhou*, K.-S. Lee, P. Liu, H.C. Tseng, and B. Cronguist, Actel Corp. *University of Toronto |
| 6:00–7:30 p.m. | DINNER, *(Dining Room)* |
| 7:30–8:30 p.m. | Announcements and Poster Session & Mixer *(Cathedral Room)*<br>Poster Session Chair: Chadwin Young, SEMATECH |
| 8:30–9:30 p.m. | **Discussion Groups:** Chair: Bill Knowlton, Boise State University ; Vice-Chair: Ricki Southwick, Boise State University<br>(One hour parallel sessions for each topic) Attendees are to participate in one of the groups |
| 9:30–10:30 p.m. | Individual SIG Meetings (to be announced at camp) |

## WEDNESDAY, October 15

7:00–8:00 a.m. BREAKFAST *(Dinning Room)*
8:00–8:15 a.m. Announcements, *(Angora Room)*
8:15–10:15 a.m. **Session #4: High-K Reliability**, Chair: William Knowlton, Boise State University
- 4.1 Effect of substrate hot carrier stress on high-k gate stack—H. Park et al., Sematech
- 4.2 Temperature (6-300K) dependence comparison of $HfO_2/SiO_2$ and $SiO_2$ MOS gate stacks—R.G. Southwick III, J. Reed, C. Buu, H. Bui, Boise State University, G. Bersuker, Sematech, and W.B. Knowlton, Boise State University
- 4.3 Positive bias temperature instability effects in advanced high-k / metal gate NMOSFETs—D.P. Ioannou et al., IBM
- 4.4 Breakdown mechanism for the thin EOT $Dy_2O_3/HfO_2$ dielectric—T. Lee et al., The University of Texas at Austin

10:15–10:30 a.m. Break
10:30–11:20 a.m. **Session #5: NBTI-2**, Chair: Jason Campbell, NIST
- 5.1 Geometry effects on the NBTI degradation of PMOS transistors—G. Math*, C. Benard* ***, J.-L. Ogier*, and D. Goguenheim ** *** * STM **ISEN-Toulon ***CNRS
- 5.2 Study of transistor and product NBTI lifetime distributions—J. Qin, B. Yan, Y. Shoshany*, D. Roy*, H. Rahamim*, and J.B. Bernstein, University of Maryland, *Freescale Semiconductor Israel

12:00–1:30 p.m. LUNCH *(Dining Room* — Take out Lunch bags available)
1:30–6:00 p.m. Open The afternoon is free for discussion, hiking & other recreation. All attendees are required to be back before darkness.
6:00–7:30 p.m. DINNER, *Dining Room*
7:30–8:30 p.m. Space Exploration and Mission Assurance—Yuan Chen, Jet Propulsion Laboratory *(Angora Room)*
8:30–9:30 p.m. **Discussion Groups:** Chair: Bill Knowlton, Boise State University ; Vice-Chair: Ricki Southwick, Boise State University (One hour parallel sessions for each topic) Attendees are to participate in one of the groups
9:30–10:30 p.m. Individual SIG Meetings (to be announced at camp)

## THURSDAY, October 16

7:00–8:00 a.m. BREAKFAST (*Dining Room*)
8:00–8:15 a.m. Announcements, *(Angora Room)*
8:15–9:30 a.m. **Session #6: Reliability of Compound Materials and Devices**, Chair: Yuan Chen, JPL
- 6.1 Interface traps in silicon carbide MOSFETs—C.J. Cochrane, P.M. Lenahan, Penn State, University, and A.J. Lelis, U.S. Army Research Laboratory
- 6.2 Effect of threshold-voltage instability on SIC DMOSFET reliability—A.J. Lelis, D. Habersat, R. Green, U.S. Army Research Laboratory, and N. Goldsman, University of Maryland
- 6.3 Coupled approach for reliability study of fully self aligned SiGe:C 250GHz HBTs—M. Diop. STM, IMEP-LAHC, N. Revil, M. Marin, F. Monsieur, T. Schwartzmann, STM and G. Ghibaudo, IMEP-LAHC

9:30–10:10 a.m. Break (Time to check out!)
10:10–11:00 a.m. **Session #7: fWLR Reliability**, Chair: Alvin Strong, IBM
- 7.1 Quantitative reliability assessment of plasma induced damage on product wafers with fast WLR measurements—A. Martin, C. Bukethal, K.-H. Rydén, S. Baier, and M. Schwerd, Infineon Technologies
- 7.2 Negative bias temperature stress on PFETs within fast wafer level reliability monitoring—R.-P. Vollertsen, H. Reisinger, and C. Schlünder, Infineon Technologies AG

11:00–12:00 p.m. **DG Summary / SIG Report / Wrap-up**
12:00–1:00 p.m. LUNCH, *(Dining Room)* & then the Workshop Ends— Attendees must Leave the Stanford Sierra Camp unless attending JC14.2

2:00 p.m. Thursday to noon Friday JEDEC 14.2 Committee on Wafer Level and Technology Reliability

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## 2008 IRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 16-17)

*Meeting registration automatically includes a room reservation.*

(Please type, print or attach business card)

NAME: ______________________
Last First Initial

COMPANY: ______________________
Mail Stop

ADDRESS: ______________________

City State/Country Zip/Postal Code

Phone: ( ______ ) ______________ Fax: ______________

Email: ______________________

For cabin assignments: ❑ male ❑ female

❑ Address is HOME

❑ Please check here if you do not wish to receive mail other than from IRW & IRPS

❑ Please check here if physically challenged and you require any auxiliary aids or services. Please call (315) 339-3971.

❑ Will bring poster. Title: ______________________

I am interested in the following Discussion Group(s):

❑ Product Reliability; ❑ NBTI; ❑ Dielectric; ❑ fWLR Monitoring

❑ My Suggestion ______________________

Method of Payment: ❑Check: Make checks payable to: **2008 IEEE/IRW**
No wire transfers ❑Credit Card: ❑AMEX ❑MASTER CARD ❑VISA ❑Diners Club

Card No. Expiration Date Signature

### REGISTRATION FEES

IEEE Member (incl. mem#__________) **$1600*** ________
NON-IEEE Member .................. **$1700*** ________
IEEE STUDENT** (mem#__________) **$ 850*** ________
**After 3-Oct-08 add late fee $100** ________

** Includes workshop attendance & handout materials, tutorial attendance, 4 nights lodging (Sun—Wed) 12 meals (dinner Sun—lunch Thurs), Final Workshop Report with CD.*
***To promote student involvement at IRW, we will be offering a reduced registration fee of $850 to the first 15 students who register. Students accepting the discount must be either IEEE member, or join the IEEE as a student member.*

### EXTRA COPIES of Workshop?

Final Report (printed) Qty:___x **$80** ________
Final Report (CD) Qty.___x **$80** ________
Final Report (printed & CD) Qty:__ x**$130** ________

JC-14.2 Mtg. accommodations*** **$400** ________
**** Includes 1 night lodging (Thursday), 3 meals (dinner Thursday— lunch Friday)*

**TOTAL REMITTED** $ ________

No wire transfers Cancellation fees: $50 after Sept. 19; full fee after Oct. 3

Send this completed form and payment to: IRW Registration; P.O. Box 308; Westmoreland, NY 13490 Paying by credit card... fax to 315-336-9134
Questions? becky@sar101.com or 315-339-3971 or web site: http://www.iirw.org

(cont. from page 2)

## DISCUSSION GROUPS

*Chair: Bill Knowlton, Boise State University*
*Vice-Chair: Ricki Southwick, Boise State University*

The evening discussion group program is a favorite highlight of the workshop experience. Attendees will have a choice of two areas on Tuesday and Wednesday evenings. The topics to be discussed will be at the discretion of those participating in the group. Each group is assigned a leader or a pair of leaders who have extensive experience with the area and will help to guide the discussion. Everyone is encouraged to bring along data and/or ideas to share on topics that are of particular interest. As we get closer to the date of the workshop, we will be surveying registered attendees so that we may prepare relevant discussion outlines to be distributed at the camp. This year's discussion areas and leaders are:

1. Product Reliability: Andrew Turner, IBM
2. NBTI: Tibor Grasser, Technical University of Vienna and Amr Haggag, Freescale Semiconductor
3. Dielectric Characterization Techniques: Chad Young, SEMATECH
4. fWLR Monitoring: Andreas Martin, Infineon Technologies AG

## SPECIAL INTEREST GROUPS

*Chair: Bill Knowlton, Boise State University*
*Vice-Chair: Ricki Southwick, Boise State University*

A Special Interest Groups (SIGs) is a collaborative working team focused on one compelling topic of mutual interest. The SIG program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. For more information on SIGs, please see http://www.iirw.org/08/08SIG.html.

## REFEREED & OPEN POSTER SESSIONS

*(Monday, and Tuesday Evenings)*
*Chair: Chadwin Young, SEMATECH*

In addition to our refereed poster sessions featured below, all attendees have the opportunity to present a poster to communicate and discuss their ideas and newest results on technical projects or issues. Please indicate in the space provided on the registration form your intention to bring a poster. A poster display board (32" x 40" or 81 cm x 100 cm) will be reserved for you. Your work should be in landscape format on 8½ x 11" or A4 paper with a maximum of twelve pages. This is a great opportunity for you to share your work with your peers. Also feel free to bring last minute results, board space will be found for you.

### Refereed Posters:

P1 Repeatability and stress level dependence on ESD-CDM testing for microelectronic components—Y. Satirakul, T. Butngam, and S. Phunyapinuant, Spansion (Thailand) Ltd

P2 Effects of pre-existing via void on electromigration reliability of Al interconnects—J.W. Pyun, J.Y. Bae, J.W. Lee, S.J. Hwang, B.H. Kwak, and W.S. Lee, Samsung Electronics

P3 Application of OTCP method for radiation-induced traps evaluation in MOS devices reliability—B. Djezzar, H. Tahi, and A. Mokrani, Microelectronics and Nanotechnologies Division of CDTA

P4 Characterization of hole and interface trapping during negative bias temperature instability (NBTI) with SiON dielectric—G. Huang, C.-Y. Kuo, V. Chiang, H.-C. Tsao, and M. Tsai, Nanya Technology Corp.

P5 Concept and implementation of an *in-situ* test structure for HTGS reliability testing of Power FETs on a wafer level basis—S. Baier, Infineon Technologies AG

P6 Fully automatical test and qualification system for a high endurance embedded EEPROM module—J. Fellner, G. Schatzberger, and A. Wiesner, austriamicrosystems AG

P7 A robust single event upset hardened clock distribution network—A.S. Mallajosyula and P. Zarkesh-Ha, University of New Mexico

P8 Reliability simulation and design consideration of high speed ADC circuits—B. Yan, J. Qin, J. Dai, Q. Fan, and J.B. Bernstein, University of Maryland

P9 Dispersion and the worst case of thermal fatigue life of solder joints in vehicle electronic devices—T. Maruoka, Q. Yu, T. Shibutani, and H. Miyauchi, Yokohama National University

P10 A comparison between V-ramp TDDB techniques for reliability evaluation—A. Aal, ELMOS Semiconductor AG

LN-P1 An electrically-detected magnetic resonance study of the atomic-scale effects of fluorine on the negative bias temperature instability—J.T. Ryan, P.M. Lenahan, Penn. State Univ., A.T. Krishnan, S. Krishnan, Texas Instruments, and J.P. Campbell NIST

LN-P2 Oxide reliability of SiC MOS devices—L. Yu, K.P. Cheung, J. Campbell, J.S. Suehle, NIST and K. Sheng, Rutgers Univ.

### Open Poster:

PO-1 A study on substrate silicon damage due to long queue time between STI trench etch & ashing using SEM, EDX and various in-line defect analysis—O.C. Nee, X-FAB

PO-2 Variations in scaled transistor parameters and their effect on advanced non-volatile memory reliability—G. Tao, NXP

PO-3 Dynamic laser stimulation for IC diagnostic—K. Sanchez, CNES

**JEDEC 14.2 Meeting.** The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is $270, which includes Thursday night dinner and lodging, and Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558, see www.jedec.org, or contact Al Strong (astrong@us.ibm.com), JC-14.2 Chair, at (802) 769-1326.

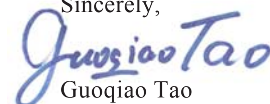
**More Information.** We expect an exciting workshop again this year. Your active participation in the many workshop activities and your active contributions to the technical discussions are key ingredients for the success of the workshop for all attendees. If you have additional questions, please contact either: me, the Technical Program Chair, Guoqiao Tao at TP.Chair@iirw.org, or the Vice Technical Program Chair, Chadwin Young at TP.VChair@iirw.org, or the General Chair, Pat Lenahan, at 814-863-4630 or General.chair@iirw.org. Web site: www.iirw.org.

*REGISTER NOW!*

Complete and send in the enclosed registration form. Please register early. We have sold out in past years. Space at the Camp limits IRW to roughly 120 attendees.

We look forward to seeing you at the Workshop!

Sincerely,



Guoqiao Tao
Technical Program Chair

# IIRW TRAVEL ARRANGEMENTS AND ACCOMMODATIONS

### ARRIVAL AT CONFERENCE CENTER (a.k.a. CAMP)

**Sunday, October 12th:** For those who are arriving on Sunday, check-in/registration does not begin until 3:00 p.m.. **Please do not arrive any earlier than 3:00 p.m.**. If you are coming later, we recommend you arrive before dark because the road from Route 89 is mostly one lane and winding.

### TRANSPORTATION

The Stanford Sierra Conference Center is located at the far end of Fallen Leaf Lake, several miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Flight arrangements into Reno can be made through the *IEEE Travel Services*. Driving time from the Reno airport to the Stanford Sierra Conference Center is approximately two hours. Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the ***South Tahoe Express.*** With a scheduled request, Stanford Sierra Conference Center will provide transportation from the Casino to the Conference Center.

### TRAVEL ARRANGEMENTS AND DISCOUNTS

Special discounted airfares for IIRW are available through IEEE Travel Services. Discounts are available with Continental Airlines. If you are flying on another carrier, contact IEEE Travel Services to check for other discounts by calling 1-800-879-4333 (US and Canada) and 1- 732-562-5387 (International) between the hours of 8:30 a.m. and 5:00 p.m. EST, Monday through Friday, or check http://www.ieeetravelonline.org and click on “Book a Flight.” This secure site offers simple and convenient service through which you can search, reserve and ticket your travel anytime, anywhere. Discounts are only available through IEEE Travel Services for air.

Special car rental rates are available with the following companies:

| Company | Code |
|---|---|
| National Car Rental | Discount Code: 5282921 |
| Avis Rental Car | Discount Code: A606098 |
| Budget Rental | Discount Code: X520000 |
| Hertz Rental | Corporate Code: 61368, Permission Code: 937661 |
| Enterprise Rental | Corporate CDP# NA24IE1 |

You may also fax or email your travel requirements including your travel dates, preferred departure and return times, and phone and fax numbers to the IEEE Travel Services; and a Travel Counselor will contact you promptly. Fax: +1 732 562 8815 ; e-mail address: travel-team@ieee.org

IEEE Travel goes the extra miles for its customers - more than today’s no-service internet travel sites. Customers receive extra benefits like: dedicated, experienced travel counselors, 24-hour emergency service, automated fare quotes, and much more!

### TRAVEL between RENO and SOUTH LAKE TAHOE

The South Tahoe Express **runs a shuttle from Reno to South Lake Tahoe** with departures from Reno on the hour from 10:00 a.m, to 7:00 p.m. and and the travel time is approximately 1½ hours. The shuttle costs $24 each way ($43 round trip) tickets can be purchased at the South Tahoe Express counter located in the baggage area in the Reno airport. Check http://www.southtahoeexpress.com/ to access the self serve ticketing system and verify schedules that are seasonal and subject to change or call 866-89-TAHOE or +1775 325-8944). The South Tahoe Express shuttle **leaves the Horizon Casino at South Lake Tahoe and returns to Reno** on the following schedule: 3:07 a.m., 5:07, 7:37, 8:37, 10:37, 12:37, 1:37 p.m., 2:37, 3:37, 5:37, and 9:37 p.m. Tickets may be purchased at the main cashier’s cage in the Horizon Casino.

### TRAVEL between SOUTH LAKE TAHOE and STANFORD SIERRA CONFERENCE CENTER (SSCC)

***You must schedule this final leg of the shuttle to the conference center at least one week before your arrival.*** SSCC offers courtesy transportation for conference attendees from the Horizon Casino between 12:30 p.m. and 11 p.m. on Registration Day (Sunday, Oct. 12). Return trips to the Casino are offered on the last day of the conference only. Notify SSCC (530-541-1244 or via internet ) at least a week prior to your arrival date. If you find yourself stranded, please call the Conference Center at the same number. The IRW Arrangements Committee may be able to provide emergency service to and from the casino. To make advance arrangements for SSCC pickup via internet: http://www.stanfordsierra.com/sitepages/pid57.php .

### ACCOMMODATIONS

The Stanford Sierra Conference Center provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note that while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. Towels and soap are provided. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks. Please be aware of the following items:

- All participants must stay at the camp during the workshop.
- We cannot accommodate spouses or any companions at the camp.
- Accommodations are not available at the Stanford Conference Center for any day before or after the workshop.
- Smoking is permitted outdoors only. Smoking is not permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3968.
- A message board will be available for incoming calls: (530) 541-1244.
- There are pay telephones for outgoing calls and there are no telephones in the rooms.
- Please have lunch before you arrive at the Conference Center, there is no lunch available on Sunday.

### RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees. Enjoy IIRW!

### WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the Conference Center. A small flashlight would be helpful to find your cabin after dark.

See http://www.iirw.org/Directions_from_Reno_Airport.htm for detailed driving directions from the Reno Airport to Conference Center.