

ESD Protection Design and Qualification Challenges

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Introduction to the topic:

ESD reliability has always been a challenge to the IC industry starting in the late 70's. Today, the advances in silicon technologies with scaling into the sub-50nm are causing a severe challenge to maintain the expected ESD performance levels for the IC components. This is compounded by the demand for high speed circuit performance which is incompatible to the capacitive and resistive parasitics introduced by the on-chip ESD protection designs. While at the same time the ESD control methods at production areas have significantly advanced to warrant a more realistic outlook for the required ESD performance levels for the component models of HBM and CDM. In addition to the component level ESD, the protection at the system board level has taken on a higher challenge. All of these considerations require a thorough understanding and a new perspective on ESD design challenges.

In this tutorial the impact of technology advances towards the 32nm and 22nm nodes on the intrinsic ESD reliability, and the trend for high speed circuit performance on the ESD protection design, will be presented in detail. These will be followed by a new perspective on the roadmap for ESD target levels.

Structure of tutorial:

The topics to be covered are

1. Basic and advanced ESD protection design techniques
2. Silicon technology scaling effects on ESD design
3. High speed and mixed voltage circuit designs and their impact on ESD performance
4. State of the art ESD control methods
5. A realistic roadmap for component level ESD
6. An overview of system board ESD protection and challenges

Who should attend:

This tutorial is aimed at technology, product, reliability and quality engineers and managers. It will give an overview of ESD design methods to meet both the technology scaling and the compatibility to advanced circuit designs. The reliability/quality engineers that attend should have a better understanding of why the ESD target levels have to be re-examined with particular attention to the recently proposed roadmap towards 22nm and beyond.

Biography of tutorial speaker:

Charvaka Duvvury is a Texas Instruments Fellow working in the Technology Design and Integration Group at Dallas. Dr. Duvvury received his Ph.D. in Engineering Science from the University of Toledo. His current work is on development and companywide support on ESD for the nanometer submicron CMOS technologies. He is internationally known and has presented many invited seminars on ESD design for semiconductor ICs. He has published over 120 papers in ESD and other IC reliability topics, co-authored four books, and holds 65 patents. He has been involved with the EOS/ESD Symposium since 1984, having served as the Technical Program Chair in 1992 and twice as the General Chair in 1994 and 2005. He has received the Outstanding Contributions Award and numerous Best Paper Awards from the EOS/ESD Symposium. Dr. Duvvury is a member of the ESDA Board of Directors since 1997, promoting university research and education in ESD. He is also an IEEE Fellow. He is a co-chair of the Industry Council on ESD Target Levels whose mission is to establish safe and realistic component ESD target levels while meeting the silicon technology challenges.