Degradation and Reliability of Metal Gate / High-k CMOS Technologies

Andreas Kerber, PhD

GLOBALFOUNDRIES, Technology Research Group,
1101 Kitchawan Rd. Yorktown Heights, NY 10598, United States
e-mail: andreas.kerber@globalfoundries.com

Introduction to the topic:
It has been demonstrated that the introduction of metal gate / high-k into CMOS technologies provides the means to-continue with traditional device gate-length scaling. The use of high-k as a new gate dielectric in combination with a metal electrode brings new reliability challenges for qualification of advanced technologies nodes not previously-encountered with conventional poly-Si / SiON gate stacks. In addition to negative bias temperature instability (NBTI) in pFET devices, positive bias temperature instability (PBTI) and stress-induced leakage currents (SILC) in nFET devices as well as dielectric breakdown are in the focus of metal gate / high-k reliability. This tutorial summarizes recent achievements towards understanding the reliability physics of metal gate / high-k CMOS devices.

Structure of tutorial:
The Tutorial will discuss BTI, SILC, and dielectric breakdown of metal gate / high-k CMOS devices and compare the behavior to conventional poly-Si / SiON gate stacks. In addition, characterization methods tailored to quantify metal gate / high-k reliability behavior will be discussed.

1. Bias temperature instability (NBTI, PBTI)
2. Stress-induced leakage current in nFET devices (SILC)
3. Dielectric breakdown
4. Outlook

Who should attend:
This Tutorial is designed for students, recent graduates, and semiconductor professionals interested in metal gate / high-k characterization and reliability. The measurement techniques discussed throughout the tutorial may also be of interest to reliability engineers in general.

Biography of tutorial speaker:

Andreas Kerber was born in Schnann, Austria, in 1973. He received his Diploma in physics from the University of Innsbruck, Austria, in 2001, where he was working at Bell Laboratories, Lucent Technologies (Murray Hill, NJ, USA) on the electrical characterization of ultra-thin gate oxides. In 2001 he joined Infineon Technologies in Munich, Germany. From 2001 to 2003 he was assigned to International SEMATECH at IMEC in Leuven, Belgium, where he was involved in the electrical characterization of alternative gate dielectrics for sub-100 nm CMOS technologies. At the same time he fulfilled the requirements for a PhD in electrical engineering and defended his thesis at the TU-Darmstadt, Germany, with honors. From 2004 to 2006 he was with the Reliability Methodology Department at Infineon Technologies in Munich, Germany, responsible for the dielectric reliability qualification of process technology transfers of 110 and 90 nm memory products. At the same time he developed a fast wafer-level data acquisition setup for time-dependent dielectric breakdown (TDDB) testing with sub-ms time resolution. In 2006 he joined AMD and now is with GLOBALFOUNDRIES in Yorktown Heights, NY, working as a Member of Technical Staff on front-end-of-line (FEOL) reliability research with focus on metal gate / high-k CMOS technologies. He has contributed to more than 50 conference and journal publications.