International *f*WLR Monitoring Guideline

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introduction to the topic: **f**ast **W**afer **L**evel **R**eliability (*f*WLR) Monitoring is a tool to monitor continuously the stability of process reliability after process qualification and the tool of choice for the assessment of **C**ontinuous **I**mprovements of the **P**rocess (CIP). Due to its advancements it is now also used as a supplement to qualification and part of the technology / process design and development flow. Measurements for single reliability items are performed in a time span of a fraction of a second up to a few seconds under highly accelerated stress conditions on a standard parametric test station. Both intrinsic (wear-out and systematic) and extrinsic (defect-based) sources of failure are addressed through stresses above use conditions. A *f*WLR Monitoring sequence consists always of initial parametric measurements, followed by some kind of reliability stress, and finally post-stress parametric measurements. Usually, testing is done on scribe line test structures on fully processed product wafers before packaging, but depending on the underlying monitoring concept level also complementary structures on short loop wafers are in use. **S**tatistical **p**rocess **c**ontrol (SPC) is employed to *f*WLR data. The assessment of *f*WLR data is usually of qualitative nature when it is included into control cards on a lot to lot basis. However, for some reliability items quantitative results can also be achieved by employing lifetime estimates or the determination of defect densities based on models which were established during process qualification.

structure of the tutorial: In this tutorial the results from numerous discussion groups and surveys between different companies are summarised and condensed. Commonly used *f*WLR methods are presented and discussed. In case of problematic reliability data a correlation to reliability failure signatures, history of root cause findings and process in-line data (tool monitors) is required and discussed in the tutorial. Furthermore, also the topics such as sampling, out of control action, raw data handling and *f*WLR data reporting are described. A general aim is to put together a *f*WLR guideline as a JEDEC publication and circulate it. The presentation will cover the topics in the following order:

- Survey of existing *f*WLR methods
- Description of most common *f*WLR methods
- Different sampling strategies
- Raw data filtering and analysis methods
- Discussion of extrinsic data characteristics and subsequent root cause finding
- *f*WLR reporting, SPC control cards
- Guideline for the interpretation of probability plots
- knowledge gain (*f*WLR ➔ qualification) ➔ new design
- Out of control action

who should attend: This tutorial presents a general overview of *f*WLR methodologies which is suitable for engineers and managers working in the area of process reliability, continuous process improvement and ZERO DEFECTS. It also addresses special stress methods for the experts in the field of process reliability testing. Since *f*WLR is differently addressed within the various affiliations the tutorial is also open to engineers who would like to discuss the presented material, controversially.

biography of tutorial speakers:

Andreas Martin received his M.Eng.Sc. in Electrical and Electronic Engineering from the Technical University of Darmstadt, Germany, in 1992. He joined the silicon technology characterisation group of the Tyndall Institute (former National Microelectronics Research Centre - NMRC), Cork, Ireland in 1992 and worked on dielectric reliability assessment and reliability simulation. Since 1998 he works for the central reliability department of Infineon Technologies AG in Munich, Germany in the field of fWLR Monitoring.
He is involved in advanced and novel test structure design, development of new stress and measurement methodologies and data analysis techniques on the topics: dielectrics, plasma induced damage, metallisation and devices. He manages PID process reliability qualifications and fWLR Monitoring pojects covering processes from 0.25µm down to 32nm for all Infineon processes worldwide.
He has published and co-authored numerous papers, and has served for many years in the management and technical committees of the IEEE IRW, IEEE IRPS and of the Workshop on Dielectrics in Microelectronics (WoDiM). He is a senior member of the IEEE, an alternate of the JEDEC subcommittee 14.2 and member of the German ITG group 8.5.6 (VDE) on WLR and reliability simulations.

Andreas Aal received his M.Eng.Sc. in Electrical and Electronic Engineering Ruhr University Bochum, Germany, in 2001. Since he joined ELMOS in 2000, he has been working on plasma-damage, failure analysis, production monitoring and process and technology qualification. Since 2005 he is the Project Manager for Process Build-in-Reliability Development at the ELMOS Semiconductor Wafer Fab, Dortmund, Germany. He is involved in the development of test structure design as well as new combined stress/measurement and data analysis methodologies for qualification and fWLR monitoring on the topics: dielectrics, plasma induced damage and metallization. He accompanies several reliability growth projects and influences process and technology design for 1.2 µm to 0.18 µm nodes for both in-house and foundry manufacturing. He has published a few papers, is a member of the IEEE and a frequent participant/contributor of the JEDEC subcommittee 14.2. Currently, he is the chair of the German ITG group 8.5.6 (VDE) on WLR and reliability simulations.