

“Reliability of gate dielectrics in MOSFETs: a nanometer scale approach with Conductive Atomic Force Microscopy”

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Introduction to the topic:

The present understanding of the electrical properties and reliability of gate dielectrics in MOSFETs has been mostly gained from the traditional current and capacitance measurements on MOS sandwich structures. The results of these studies represent the oxide properties typically averaged over areas 10^{-8} - 10^{-3} cm² and do not necessarily reflect sample variations on a nanometer scale. However, with the ongoing reduction of device dimensions, local fluctuations in the oxide properties become increasingly important, so that characterization tools with larger spatial resolution are required to investigate its properties at the nanoscale. In this direction, Atomic Force Microscopy (AFM) based techniques can provide electrical information with resolution of atomic dimensions. When working on bare gate dielectric surfaces, the conductive tip of the AFM plays the role of the gate electrode of a MOS structure whose size is mainly determined by the tip-sample contact region, which has been estimated to be of only several hundreds of nm². Therefore, the gate dielectric can be electrically characterized in detail, revealing aspects that can be hidden by standard electrical tests.

In this tutorial, an overview of the use of AFM based techniques for gate oxide reliability evaluation, with emphasis on the influence of the experimental details, will be done. The main results obtained on the electrical characterization and aging mechanisms of SiO₂ and high-k stacks at nanometer scale will be presented, when using Conductive Atomic Force Microscopy.

Structure of tutorial:

The tutorial will be mainly focused on the reliability evaluation of ultrathin gate dielectrics (SiO₂ and high-k stacks) in MOSFETs with Conductive Atomic Force Microscopy. The topics that will be covered are:

1. Introduction: the need of nanoscale characterization.
2. Overview of Scanning Probe Microscopies: the Atomic Force Microscope and related tools.
3. CAFM evaluation of SiO₂ reliability at the nanoscale.
4. Improvement of the CAFM technique: high-k gate stacks reliability.

Who should attend:

The tutorial is aimed at participants with a background on the electrical characterization and reliability of MOSFETs who want to get knowledge on the possibilities that Scanning Probe Microscopies offer for the electrical characterization of gate dielectrics at the nanoscale. A better understanding of the details of their aging mechanisms will be gained.

Biography of tutorial speaker:

Montserrat Nafria received the Ph.D. in Physics in 1993 from the Universitat Autònoma de Barcelona, where, currently, she is an Associate Professor at the Department of Electronic Engineering. Her major research interest is in the area of CMOS devices and circuits reliability. Currently, she is working on the reliability of high-k dielectric based MOS devices, including their nanoscale characterization using AFM related techniques and the modelling of gate dielectric related failure mechanisms (breakdown, BTI, hot carriers) for circuit reliability simulation. She has (co)authored more than 150 research papers in scientific journals and conferences in all these fields.