

2011 IEEE International Integrated Reliability Workshop 30th anniversary



October 16-20, 2011

<http://www.iirw.org>

Stanford Sierra Conference Center, S. Lake Tahoe, CA

CALL FOR PAPERS

Abstract Submission Deadline: *July 16, 2011*

In 2011, the IIRW that originated from the Wafer Level Reliability Workshop celebrates its 30th anniversary ! The committee is honored to announce the return of O. D. "Bud" Trapp who initiated the Workshop in 1982. Bud will give a special Sunday Night Talk on the unique history of IIRW. We understand participation in standards development is a necessary aspect for the advancement of semiconductors as well as a common role for many semiconductor reliability professionals to participate in the development of these standards. Therefore, IIRW is taking another step forward and will integrate selected JEDEC sessions into the IIRW 2011 program itself.

Generally, the IIRW focuses on ensuring electronic device reliability through fabrication, design, testing, characterization, and simulation, as well as identification of the defects and physical mechanisms responsible for reliability problems. Through tutorials, paper presentations, discussion groups, special interest groups, and the informal format of the technical program, a unique environment is provided for understanding, developing, and sharing reliability technology and test methodology for present and future semiconductor applications as well as ample opportunity for discussions and interactions with colleagues.

Hot reliability topics for the workshop include: SiGe and strained Si, III-V, SOI, high- κ and nitrided SiO₂ gate dielectrics, reliability assessment of novel devices, organic electronics, emerging memory technologies and future "nano"-technologies, NEMS/MEMS, photovoltaics, transistor reliability including hot carriers and NBTI/PBTI, Cu interconnects and low- κ dielectrics, product reliability and burn-in strategy, impact of transistor degradation on circuit reliability, reliability modeling and simulation, optoelectronics, single event upsets.

We invite you to submit a presentation proposal that addresses any semiconductor related reliability issue, including the following topics:

- Designing-in reliability (products, circuits, systems, processes)
- Identification and characterization of reliability effects
- Deep sub-micron transistor and circuit reliability
- Customer product reliability requirements / manufacturer reliability tasks
- Root cause defects, physical mechanisms, and simulations
- Wafer level reliability tests, test approaches, and reliability test structures

Abstract submission: Your *two-page extended abstract* (maximum two pages including figures) should state clearly and concisely the results of your work and why they are significant. Representative data and figures that support your proposal are REQUIRED.

Please e-mail your abstract to the Technical Program Chair, no later than *July 16, 2011*, either as an MS Word document or pdf attachment. A final version of the accepted papers is due at the workshop for inclusion in the Final Report published by IEEE.

For more information, please visit: WWW.IIRW.ORG or contact the Technical Program Chair: Andrew Turner: aaturner@us.ibm.com, Tel: 802.769.6140