

# 2011 IEEE International Integrated Reliability Workshop

## PROGRAM SCHEDULE

**SUNDAY, October 16** Please have lunch before arriving at the camp; no lunch will be served at the camp.

- 3:00–6:00 p.m. Registration: Pick up badges & handout (*Lodge Lounge*)  
Discussion Group and SIG Signup; Poster preparation
- 3:00–8:00 p.m. Lodge check-in. Get room assignment (prearranged) & room key.  
(If physically challenged please notify desk of special needs.)
- 6:15–7:30 p.m. DINNER, (*Dining Room*) authors: dine with your session chair
- 7:30–9:00 p.m. **Invited Talk:** History of IIRW—Bud Trapp, Founder WLRW

### MONDAY, October 17

- 7:00–8:00 a.m. BREAKFAST (*Dining Room*)
- 8:05–8:30 a.m. (Angora Room) Welcome & Introduction: Rolf Geilenkeuser, General Chair; Drew Turner, Technical Program Chair
- 8:30–9:30 a.m. **Keynote:** Scaling to the Final Frontier: Reliability challenges in sub 20 nm technologies—Tanya Nigam, GLOBALFOUNDRIES
- 9:30–9:40 a.m. Break
- 9:40–11:40 a.m. **Session #1: Bias Temperature Instability**, Chair: Tibor Grasser, TU Wien (*Angora Room*)
- 1.1 (Invited) Separating NBTI and PBTI effects on the Degradation of Ring Oscillator Frequency—B.P. Linder, J.-J. Kim, A. Bansal, R. Rao, K. Jenkins, IBM T.J. Watson Research Center
  - 1.2 On the PBTI degradation of pMOSFETs and its impact on IC lifetime—C. Schlünder, H. Reisinger, S. Aresu, W. Gustin, Infineon Technologies AG
  - 1.3 Cryogenic to room temperature effects of NBTI in high-k PMOS devices—R.G. Southwick III<sup>1,2</sup>, S.T. Purnell<sup>1</sup>, B.A. Rapp<sup>1</sup>, R.J. Thompson<sup>1</sup>, S. K. Pugmire<sup>1</sup>, B. Kaczer<sup>3</sup>, T. Grasser<sup>4</sup>, W.B. Knowlton<sup>1</sup>  
<sup>1</sup>Boise State University <sup>2</sup>NIST, <sup>3</sup>IMEC, and <sup>4</sup>Technische Universität Wien
  - 1.4 On the Microscopic Limit of the Reaction-Diffusion Model for the Negative Bias Temperature Instability—F. Schanovsky, T. Grasser, TU Wien
- 11:40–12:00 p.m. AUTHOR'S CORNER
- 12:00–1:00 p.m. LUNCH, (*Dining Room*)
- 1:00–2:30 p.m. **Tutorial #1:** Charge Pumping: an overview of the technique and recent new features—Daniel Bauza, IMEP-LAHC
- 2:30–3:45 p.m. **Session #2: DEVICES**, Chair: Patrick Lenahan, Penn State University (*Angora Room*)
- 2.1 (Invited) Technology variability and product design implications—David M. Fried, IBM Systems & Tech. Group
  - 2.2 Experimentally Based Methodology for Charge Pumping Bulk Defect Trapping Correction—J.T. Ryan, R.G. Southwick, J.P. Campbell, K.P. Cheung, C.D. Young\*, and J.S. Suehle, NIST \*SEMATECH,
  - 2.3 Modeling of DCIV Recombination Currents Using A Multistate Multiphonon Model—M. Bina, Th. Aichinger\*, G. Pobegen\*\*, W. Göes, and T. Grasser, TU Wien \*Penn State University, \*\*KAI
- 3:45–4:05 p.m. Break/Author's Corner
- 4:05–5:35 p.m. **Tutorial #2:** Reliability of Poly-Si and IGZO TFTs—Ryoichi Ishihara, Delft University of Technology
- 6:00–7:30 p.m. DINNER, (*Dining Room*) authors: dine with your session chair
- 7:30–8:30 p.m. **Poster Session** (*Cathedral Room*), Chair: Tibor Grasser, TU Wien
- 8:30–10:00 p.m. Mixer

### TUESDAY, October 18

- 7:00–8:00 a.m. BREAKFAST (*Dining Room*)
- 8:05–8:15 a.m. Announcements (Angora Room)
- 8:15–9:45 a.m. **Tutorial #3:** Reliability assurance and process control for products walking at the edge of the abyss—Tim Turner, College of Nano-scale Science and Engineering
- 9:45–10:00 a.m. Break
- 10:00–11:25 a.m. **Session #3: CIRCUITS**, Chair: Drew Turner, IBM (*Angora Room*)
- 3.1 (Invited) Recent trends in CMOS reliability: from individual traps to circuit simulations—B. Kaczer<sup>1</sup>, M. Toledano-Luque<sup>1</sup>, J. Franco<sup>1,2</sup>, T. Grasser<sup>3</sup>, Ph. J. Roussel<sup>1</sup>, V. V. A. Camargo<sup>4</sup>, S. Mahato<sup>2</sup>, E. Simoen<sup>1</sup>, F. Catthoor<sup>1,2</sup>, G.I. Wirth<sup>4</sup>, G. Groeseneken<sup>1,2</sup> <sup>1</sup>imec (Belgium); <sup>2</sup>KULeuven (Belgium); <sup>3</sup>TU Wien (Austria); <sup>4</sup>UFRGS (Brazil)
  - 3.2 When Does a Circuit Really Fail?—J.T. Ryan, L. Wei<sup>1</sup>, J.P. Campbell, R.G. Southwick, K.P. Cheung, A.S. Oates<sup>2</sup>, H.-S.P. Wong<sup>3</sup> and J. Suehle, NIST <sup>1</sup>MIT, <sup>2</sup>TSMC, <sup>3</sup>Stanford University
- 11:25–11:40 p.m. Break/Author's Corner
- 11:40–12:00 p.m. Group Picture
- 12:00–1:00 p.m. LUNCH, *Dining Room*
- 1:15–2:25 p.m. **Tutorial #4:** New Methodologies for Reliability Testing and Analysis: GaN Electronic Devices - Beyond Arrhenius—Martin Kuball, University of Bristol

2:25–3:15 p.m. **Session #4: III-V DEVICES**, Chair: Todd Weatherford, Naval Postgraduate School (*Angora Room*)

- 4.1 Reliability Analysis of Enhancement-Mode GaN MIS-HEMT with Gate-Recess Structure for Power Supplies—T. Imada, K. Motoyoshi, M. Kanamura, T. Kikkawa, Fujitsu Laboratories Ltd.
- 4.2 Reliability and degradation mechanism of 0.25  $\mu\text{m}$  AlGaIn/GaN HEMTs under rf stress conditions—M. Dammann, M. Baeumler, F. Gütle, M. Cäsar, H. Walcher, P. Waltereit, W. Bronner, S. Müller, R. Kiefer, R. Quay, M. Mikulla, O. Ambacher, A. Graff, F. Altmann, M. Simon, Fraunhofer Institute

3:15–3:35 p.m. Break/Author's Corner

3:35–5:05 p.m. **Tutorial #5:** Ghosts in the machine – how subatomic-scale events impact us and what we can do about it—Robert Baumann, Texas Instruments

5:05–5:25 p.m. (Invited) JEDEC: JC 14.2 Wafer Level Reliability Standards Activity—Tim Sullivan, IBM

6:00–7:00 p.m. DINNER, (*Dining Room*)

7:00–8:30 p.m. **Discussion Groups:** Chair: Jim Lloyd, SUNY CNSE Albany  
(90 minute parallel sessions for each topic) Attendees are to participate in one of the groups

8:30–10:00 p.m. **SIGs:** Chair: Jim Lloyd, SUNY CNSE Albany

## WEDNESDAY, October 19

7:00–8:00 a.m. BREAKFAST (*Dining Room*)

8:05–8:15 a.m. Announcements, (*Angora Room*)

8:15–9:15 a.m. **Tutorial #6:** New Architectures for Non Volatile Semiconductor Memory Scaling and related reliability issues—Salvatore Lombardo, CNR-IMM

9:15–9:40 a.m. **Session #5: MEMORY**, Chair: Guoqiao Tao, NXP Semiconductors (*Angora Room*)

- 5.1 User Verify and Disturb Mechanisms in a 65nm Flash FPGA—J.Y. Jia, P. Singaraju, F. Dhaoui, R. Newell, P. Liu, H. Micael, M. Traas, S. Sammie, J.J. Wang, F. Hawley, J. McCollum, W. van den Abeelen, E. Hamdy, C. Hu\*, Microsemi Corporation \*University of California at Berkeley

9:40–10:00 a.m. Break/Author's Corner

10:00–11:40 a.m. **Session #6: BEOL**, Chair: Barry O'Connell, Fairchild Semiconductor (*Angora Room*)

- 6.1 Electron Spin Resonance Studies of Interlayer Dielectrics—B.C. Bittel, T.A. Pomorski, P.M. Lenahan, and S.W. King
- 6.2 Constant Voltage Electromigration Testing—J.R. Lloyd, N. Connelly, Z. Zhang, M. Rizzolo, SUNY Albany CNSE
- 6.3 Effects of current density on electromigration resistance trace analysis—F. Bana<sup>1,2</sup>, D. Ney<sup>1</sup>, L. Arnaud<sup>3</sup>, R. Galand<sup>1,2</sup>, Y. Wouters<sup>2</sup> <sup>1</sup>ST Microelectronics <sup>2</sup>SiMaP <sup>3</sup>CEA-Leti Minatec
- 6.4 Inline Process Characterization and Control for Robust BEOL Reliability—Y.C. Ee, W.L. Ng, J.B. Tan, F. Zhang, W. Shao, J.K. Chua, H.X. Li, B.F. Lin, C.W. Ng, E. Ramanathan, GLOBALFOUNDRIES Singapore Pte. Ltd

12:00–1:30 p.m. LUNCH (*Dining Room* — Take out Lunch bags available)

1:30–6:00 p.m. Open The afternoon is free for discussion, hiking & other recreation. All attendees are required to be back before darkness.

6:00–7:30 p.m. DINNER, (*Dining Room*)

7:30–8:30 p.m. **Poster Session** (*Cathedral Room*), Chair: Tibor Grasser, TU Wien

8:30–9:30 p.m. **Discussion Groups:** Chair: Jim Lloyd, SUNY CNSE Albany  
(60 minute parallel sessions for each topic) Attendees are to participate in one of the groups

9:30–10:30 p.m. **Individual SIG Meetings** (to be announced at camp)

## THURSDAY, October 20

7:00–8:00 a.m. BREAKFAST (*Dining Room*)

8:05–8:15 a.m. Announcements, (*Angora Room*)

8:15–9:30 a.m. **Session #7: HOT CARRIERS**, Chair: Andreas Martin, Infineon Technologies AG (*Angora Room*)

- 7.1 Effects of Pre-Stress on Hot-Carrier Degradation in N-Channel MOSFETs—T. Kopley, B. O'Connell, National Semiconductor
- 7.2 An advanced RF-CV method as a powerful characterization tool for the description of HC induced defect generation at microscopic level—L. Negre<sup>1,2</sup>, D. Roy<sup>2</sup>, P. Scheer<sup>2</sup>, D. Gloria<sup>2</sup>, G. Ghibaud<sup>1</sup> <sup>1</sup>IMEP-LAHC <sup>2</sup>STMicroelectronics
- 7.3 Hot-Carrier and Recovery Effect on p-channel Lateral DMOS Transistors—S. Aresu, R.-P. Vollertsen, R. Rudolf, C. Schlünder, H. Reisinger, Infineon Technologies AG

9:30–10:20 a.m. **Session #8: fWLR/TDDb**, Chair: Bill Knowlton, Boise State University (*Angora Room*)

- 8.1 Reliability Degradation of MOS Transistors Originated from Plasma Process-Induced Charging of Circuit Blocks and Detected with fWLR Methods—A. Martin, C. Wagner, A. Kotten, Infineon Technologies AG
- 8.2 TDDb characterization of BST capacitors exhibiting bimodal Weibull distributions—H. Lin<sup>1,2</sup>, E. Bouyssou<sup>1</sup>, L. Ventura<sup>2</sup> <sup>1</sup>STMicroelectronics <sup>2</sup>François Rabelais University

10:20–10:45 a.m. Author's Corners/Break/Time to check out!

10:45–11:35 a.m. **Session #9: LATE NEWS**, Chair: Jason Campbell, NIST

11:35–12:00 p.m. **DG Summary / SIG Report / Wrap-up**

12:00–1:00 p.m. LUNCH, (*Dining Room*) & then the Workshop Ends— Attendees must leave the Stanford Sierra Camp

NOTE: JC-14.2 meeting starts at 1:00 p.m. at Inn By The Lake, South Lake Tahoe