

Charge Pumping: an overview of the technique and recent new features

A tutorial presented by:

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Abstract:

Charge pumping (CP) is a well-known technique for electrical characterization of semiconductor-insulator interface traps. It has been proposed more than four decades ago and applies primarily to MOSFETs as it requires the switching of the device between inversion and accumulation. Until now, it has therefore been mainly used to study the Si-SiO₂ system and accompanied MOSFET scaling.

The charge pumping current results from recombination of minority carriers stored in inversion in the semiconductor-insulator interface traps with majority carriers coming from the substrate when switching the device in accumulation. The charge that recombines therefore flows from source and drain, generally connected together and grounded, toward the substrate. Repeating this single recombination process using a gate signal with a given frequency provides a net DC current which can be measured and is at first order proportional to the signal frequency.

Today, CP remains a technique of choice for characterizing interface traps in MOSFETs. This is true not only in the case of silicon devices with high- κ gate dielectrics but also in the case of MOSFETs realized on high mobility substrates which become topical.

This tutorial will introduce the charge pumping technique. It will aim at providing an overview of the characteristics of the method, of some of its applications and of its limitations. The CP mechanisms, the traps probed and how the technique interacts with the trap properties will be dealt with. Parasitic effects that may impact the CP signal and the way they can be detected and minimized will be detailed. Adaptation of the technique to MOSFET scaling will be discussed. Its use for studying traps in transistors with high- κ gate stacks as well as in MOSFETs realized on high mobility substrates will also be presented.

Author Biography:

Daniel Bauza is a CNRS researcher at the IMEP-LAHC, MINATEC-Grenoble-France. He received a MS and a PhD degree from the University of Paris XII, France in 1982 and 1986, respectively. His research interests are on the electrical characterization of defects in semiconductor devices and on the development of electrical characterization tools to better understand the electrical measurements carried out and extract trap properties. He has authored or co-authored over 70 papers in journals or international conferences and four book chapters. He holds an H.D.R. (academic research supervisor).

OUTLINE OF THE PRESENTATION

Introduction

- 1 - CP principle and primary approach
- 2 - Shockley-Read-Hall kinetics
- 3 - CP: Toward a better understanding
- 4 - Other gate signals used
- 5 - Study of the energy region probed
- 6 - Other contributions to I_{cp}/Q_{cp}
- 7 - CP: Toward a better understanding
- 8 - CP curves simulation
- 9 - Deep Submicron area devices
- 10 - Devices with ultrathin silicon oxide
- 11 - High- κ gate stacks on silicon devices
- 12 - MOSFETs on high mobility substrates

Conclusion