

New Architectures for Non Volatile Semiconductor Memory Scaling and Related Reliability Issues

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Scaling of Flash memories is constantly posing new challenges so new device architectures are now seen with large interest. The basic floating gate Flash transistor cell is based on a vertical stack consisting in a control gate, an interpoly dielectric (IPD), the floating gate made of polysilicon, a tunnel dielectric, and the silicon channel. Tunnel dielectric must be thin enough to allow charge transfer at reasonably low voltages but thick enough to avoid charge loss during read or in off mode. Similar retention requirement has to be satisfied by the IPD. Retention has to be satisfied after extensive memory cell program / erase cycling and also at high temperature. Because of these requirements, both tunnel dielectric and IPD have scaled very slowly through Flash memory evolution. In the first part of the talk these basic Flash reliability aspects will be reviewed.

Given the constraints on the tunnel and IPD thickness reduction, the Flash scaling presents a major problem in maintaining a sufficiently high gate coupling ratio (GCR). For this purpose the control gate wraps the floating gate to provide extra capacitance, but this technique cannot be pursued as the memory half pitch is scaled well beyond 32 nm, being the IPD thickness of 10-15 nm. In addition, fringing field effect and floating-gate interference effects pose further formidable challenges. So a number of new approaches have been taken into consideration. The first are variations of the basic SONOS concept. Instead of using a floating gate, the charge is trapped in electronic defects of silicon nitride thin films. This eliminates the issues of gate coupling ratio and of neighboring cell cross talk. Basic SONOS however presents a major limitation, i.e. a very thin tunnel dielectric, necessary to allow erase, but with a corresponding insufficient charge retention. This limit can be overtaken by various approaches: one is the use of the NROM concept, of great success in the area of NOR-type Flash products. Another is charge storage in silicon quantum dots or in metallic dots; another is to use tunnel dielectric engineering concepts to modify the tunneling barrier properties to create "variable thickness" tunnel dielectrics. Another approach is to use MANOS (metal-Al₂O₃-nitride-oxide-Si) gate stacks, in which a high- κ blocking dielectric and metal gate are combined to prevent gate injection during erase. Other advantages are obtained by using non-planar and multi-gate devices such as FinFET, which allow better channel control and allow further scaling. These device structures will be discussed in the second part of the talk, with focus on the relevant physics concerning their operation and reliability issues (program / erase mechanisms, retention, endurance).

Since even these new devices are ultimately limited by the number of electrons stored per bit, novel approaches based on non-charge-based NVM cells are being heavily investigated. Among these there is the phase change memory, based on the reversible amorphous-crystal phase transition in a small volume of a chalcogenide material. The basic physics of this type of cell and the possible materials to be used for the phase change will be reviewed in the final part of the talk, with an overview of the basic reliability limits.

Author Biography

Salvatore A. LOMBARDO received a B.S. (cum laude) and a Ph.D. in Physics from the University of Catania, Italy, in 1989 and in 1994, respectively. He joined the Italian National Research Council (CNR) in 1994 and in the period 2001-2010 he was Senior Scientist of CNR at the IMM Institute. From 2010 he is Research Manager of CNR at the IMM Institute. He has spent various periods as visiting scientist at Cornell University, IBM-Research, and STMicroelectronics. His research interests are in the field of semiconductor devices and electronic materials. Dr. Lombardo is committee member and served as chair of numerous international workshops and conferences. He was involved in the coordination of several R&D national and European projects and of scientific collaborations with USA, Singapore, and Israel institutions. He is author of 7 patents, 5 review articles, and of about 200 scientific and technical papers published on international journals.