

Reliability Assurance and Process Control for Products walking at the edge of the Abyss

A tutorial presented by:

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Abstract:

In the early days of semiconductor manufacturing, products were built with wafer yields that might be as low as 40%. The high defect density on these products created a huge infant mortality problem that dominated the reliability concerns at that time. Back then, power dissipation did not limit circuit density or speed and the materials involved were primarily Si, SiO₂ and Al. The semiconductor world is much different today, but many of the reliability control programs developed for that world, are still used today.

In the days when defect densities generated infant mortality defects and the material lifetime was hundreds or even thousands of years, a product based operating life test made sense as the primary reliability monitor. Unfortunately, we are not still limited to Si, SiO₂ and Al. New materials have been added to our material set. Reliability has been one of the biggest hurdles in the development of these new materials. Development continued until we could meet the minimum lifetime rules for these materials, then it stopped. This leaves us with little margin for error.

At the same time, the industry has made great strides in reducing the defect density. We now see 300mm wafers with one or two bad die per wafer. Reliability process variation is now less likely to produce an infant mortality problem and more likely to produce early wear-out. A 1,000 hour life test is generally insensitive to wear-out lifetime degradation. This insensitivity is increased by specs which allow a few defects without regard for the point in time where they occurred.

This tutorial will describe techniques for monitoring the reliability of state of the art semiconductor products. A program will be described that will enable the detection and elimination of future problems, not just existing problems. Like everything in the semiconductor industry, this program will require more technology, combining simulation, testing and statistical techniques to obtain higher performance without higher costs.

Author Biography:

Tim Turner is a researcher at the SUNY College of Nanoscale Science and Engineering in Albany, NY. He has more than 35 years of experience in Semiconductor Reliability assurance at Mostek, ST Microelectronics, Keithley Instruments and Texas Semicon Labs. Mr. Turner was the first to describe and model Stress Migration and was an early pioneer in the field of Wafer Level Reliability.