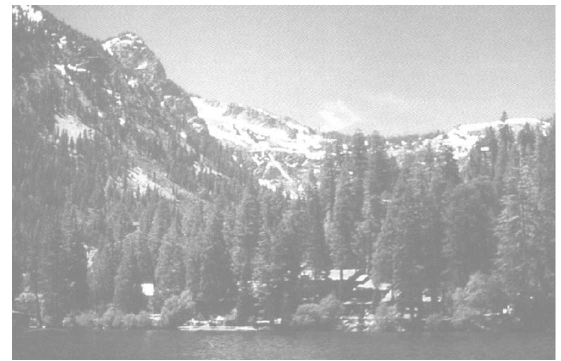
1996 *International*

INTEGRATED RELIABILITY WORKSHOP



October 20-23, 1996

Stanford Sierra Camp, Lake Tahoe, CA

CALL FOR PAPERS

Since 1982, the Integrated Reliability Workshop and its predecessor, the Wafer Level Reliability Workshop, have provided a unique forum for sharing new approaches to achieve and maintain microelectronic component reliability. The Workshop features presentations, tutorials, open poster sessions, moderated discussion group sessions, and special interest group (SIG) meetings. All Workshop activities take place in a relaxed and rustic setting that promotes interactive learning and knowledge sharing.

Aggressive cost, reliability, and market entry demands are forcing the semiconductor industry to consider alternatives to the traditional and increasingly inadequate approach of testing-in-reliability (e.g., burn-in, life test). In response to these concerns, the Workshop is continuing to highlight the need for an integrated approach to ensure product reliability, in which a detailed understanding of potential failure mechanisms and their sources are proactively incorporated into robust design and manufacturing practices. The four topical areas for this year's Workshop reflect the scope of this approach and serve as a framework for exploring solutions.

We invite you to submit a presentation proposal that addresses one or more of the following topics:

- **PHYSICS OF THE FAILURE**

  Fundamental investigations into potential failure mechanisms, their sources, and methods of activation.
  - Role of chemical, electrical, mechanical, or thermal processes leading to failure
  - Product or device geometry, materials, and manufacturing sensitivities that contribute to failure
  - Failure mechanisms in new and emerging technologies
  - Reliability models

- **RELIABILITY TEST STRUCTURES**

  This new topic for 1996 has been added in response to numerous requests from attendees. Test structures are fundamental tools for investigating and monitoring potential failure mechanisms. Presentations of a tutorial nature will also be considered.
  - Reliability test structure design, characterization, and analysis
  - New test procedures
  - Failure-mechanism-specific test structures
  - Customized test structures (e.g., package / die interaction)
  - Active test structures (e.g., self-stressing / self-heating)
  - Defect arrays / addressable test structures

- **WAFER LEVEL RELIABILITY (WLR)**

  In-line or end-of-line reliability measurements for manufacturing control verification and early detection of specific reliability problems.
  - Examples of WLR programs and infrastructure
  - New or novel WLR test methodologies, analysis techniques
  - In-process monitors for early problem detection / correction
  - WLR program problem detection / reliability correlation examples

- **BUILDING-IN-RELIABILITY (BIR)**

  A methodology for eliminating causes of product failures through proactive reliability engineering integrated throughout the design, process, and assembly disciplines and utilized throughout all phases of product conception, development, and manufacturing.
  - Integration of reliability models into process, device, circuit, and packaging simulation tools
  - Reliability-driven rules for design, devices, processes, and manufacturing equipment
  - Characterizing and designing to the product usage environment and process capability
  - Qualifying and controlling the product manufacturing, assembly, and maintenance processes
  - New approaches to product reliability assessment; the vendor/customer partnership

SUBMISSION DEADLINE: ***July 15, 1996*.**

Please submit 15 copies of your two-page presentation proposal (including figures and 0.75" margin on all sides). Your submission should state clearly and concisely the results of your work and why they are significant. Representative data or figures that support your proposal are REQUIRED. The proposal must include the title of the presentation, and the name, affiliation, complete return address, telephone and telefax numbers, and e-mail address for each author. Submission should be by post or express mail and NOT telefax. All submissions will be acknowledged. Visual aids for accepted proposals are required by *September 27, 1996* for inclusion in the Presentation Handout at the meeting. A written presentation summary will be due by *December 13, 1996* for inclusion in the Final Report.

MAIL TO: James W. Miller, Technical Program Chair, 1996 IRW
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ADVANCE REGISTRATION

Advance Registration should be made now to insure your space at the Workshop.

THE WORKSHOP HAS LIMITED SPACE AND YOU ARE ENCOURAGED TO REGISTER EARLY.

The Registration fee is US$875 for IEEE Members and US$950 for non-members, which includes: meals, lodging, and refreshments at the Stanford Sierra Camp; Presentation View Graphs (provided at the Meeting); and the 1996 IRW Final Report (published after the Meeting).

LODGING & FACILITIES

Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, a few miles from South Lake Tahoe, are clusters of 2 and 3 bedroom cabins furnished in the rustic style of an alpine resort. Each cabin cluster is equipped with shared bathroom facilities. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

The physical isolation of the location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees.

Lodging is available for meeting attendees only.

JEDEC 14.2 MEETING

The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Wednesday afternoon and all day Thursday. Members, alternates, and guests are welcome. The cost for the accommodations is $160.00, which includes Wednesday night dinner and lodging *and* Thursday breakfast and lunch. Accommodations at the camp will not be available for Thursday night. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558.

INTEGRATED RELIABILITY WORKSHOP ADVANCE REGISTRATION FORM

(Please type, print or attach business card)

NAME: ______________________ TITLE: ______________
Last First Initial

COMPANY: ______________________________ Mail Code

ADDRESS: ______________________________

City State/Country Zip/Postal Code

PHONE: (_____) ______________ FAX: ______________

EMAIL: ______________________________

☐ Address is HOME, Company not to be included on mailing label

☐ Please check here if you do not wish to receive mail other than from IRW & IRPS

☐ Please check here if under the Americans With Disabilities Act, you require any auxiliary aids or services. Please call (315) 339-3971.

For cabin assignments: ☐ male ☐ female

ADVANCE REGISTRATION FEES

IEEE Member ____________ .. **$875*** _______
(member No. Req'd)

NON-IEEE Member .... **$950*** _______

** Includes meals, lodging, Handout, & Final Report. (Sun. eve., Oct. 20- Wed. noon, Oct. 23)*

EXTRA COPIES of Workshop Final Report ..... Qty: ______ x **$80** _______

JC14.2 accommodations .... **$160** _______

TOTAL REMITTED $ _______

Please note that meeting registration automatically includes a room reservation.

MAKE CHECKS PAYABLE TO
"IEEE INTEGRATED RELIABILITY WORKSHOP"

SEND REGISTRATION FORM TO:

Intl. Integrated Reliability Workshop
P.O.Box 308
Westmoreland, NY 13490-0308

For registration information:
Phone: 315-339-3971
FAX: 315-336-9134
email: 103227.2074@compuserve.com

HISTORY

The Wafer Level Reliability Workshop was initiated in 1982 through the efforts of O. D. "Bud" Trapp, of Technology Associates, and the active support and encouragement of DARPA (Defense Advanced Research Projects Agency). This support continued for the first eight years of the Workshop and included active support and involvement of the Stanford University Integrated Circuits Laboratory and the University of California, Berkeley, Dept. of Electrical Engineering and Computer Sciences. After DARPA sponsorship ended, Bud Trapp continued the direction of the Workshop until 1991 after which time he requested that sponsorship and management be assumed by an appropriate professional association. The IEEE accepted this responsibility in 1992. In 1993, the name of the Workshop was changed to the Integrated Reliability Workshop. This change reflects the enlarged scope of the Workshop, the integrated nature of reliability in the manufacture of semiconductor products, and the need for a broader and a more comprehensive approach to reliability engineering.

SPONSORS

The International Integrated Reliability Workshop is sponsored and managed by the IEEE Electron Device Society and the IEEE Reliability Society through the Board of Directors of the International Reliability Physics Symposium.