2013 IEEE International Integrated Reliability Workshop

PROGRAM SCHEDULE

SUNDAY, October 13  Please have lunch before arriving at the camp; no lunch will be served at the camp.
3:00–6:00 p.m.  Registration: Pick up badges and handout, Discussion Group and SIG Signup (Lodge Lounge)
3:00–8:00 p.m.  Lodge check-in. Get room assignment (prearranged) & room key. (If physically challenged please notify desk of special needs.)
6:15–7:30 p.m.  DINNER, (Dining Room)
7:30–8:30 p.m.  Invited Talk: (Sunday Night Tutorial) The Magic of Lasers in Entertainment – Behind the Technology—John Suehle, NIST

MONDAY, October 14
7:00–8:00 a.m.  BREAKFAST (Dining Room)
8:05 a.m.  Session #1 (Angora Room)
8:05–8:10 a.m.  Welcome & Introduction—General Chair: Jason Campbell, NIST
8:10–8:20 a.m.  Technical Program Overview—Technical Program Chair: Tibor Grasser, TU Wien,
9:20–9:55 a.m.  1.1 (INVITED) Atomic Scale Defects in MOS Reliability Problems—Pat Lenahan, Penn State University
9:55–10:30 a.m.  1.2 (INVITED) Radiation Effects and Reliability: Physical Mechanisms and Rate Prediction—Ron Schrimpf, Vanderbilt University
10:30–10:50 a.m.  Coffee Break

Session #2 (Angora Room)
10:50–11:25 a.m.  2.1 (INVITED) Reliability Concerns of Yesterday – Emerging Memory Cells of Tomorrow?—Chandra Mouli, Micron
11:25–12:00 p.m.  2.2 (INVITED) If Interconnects do not Scale with Advancing Technology, What is There to say about Reliability?—Ennis Ogawa, Broadcom
12:00–1:00 p.m.  LUNCH, (Dining Room)
1:00–2:05 p.m.  Tutorial #1: Mechanisms and Performance of Metal Oxide Resistive RAM (RRAM)—An Chen, Globalfoundries

Session #3 (Angora Room)
2:05–2:40 p.m.  3.1 (INVITED) Recent Advances in Dielectric Breakdown of Modern Gate Dielectrics—Ernest Wu, IBM
2:40–3:00 p.m.  3.2 New Insight on the Frequency Dependence of TDDB in High-k/Metal Gate Stacks—Anas Bezza, Mustapha Rafik, David Roy, Xavier Federspiel, Pascal Mora, STMicroelectronics, Gerald Ghibaudo, IMEP (UMR CNRS/INPG/UJF)
3:00–3:20 p.m.  3.3 Electrical Stressing of HfO2/Al2O3 Bilayer Metal-Insulator-Insulator-Metal Diodes—Tyler Klarr, Dustin Austin, Nasir Alamdarni, John Conley, Oregon State University
3:20–3:40 p.m.  Coffee Break

Session #4 (Angora Room)  Characterization
3:40–4:15 p.m.  4.1 (INVITED) Degradation and Reliability of Silicon Power Transistors—Jurriaan Schmitz, University of Twente
4:15–4:50 p.m.  4.2 (INVITED) Assessing the Reliability and Performance Impact on the Three-Dimensional Structure of Multigate Field Effect Transistor (MugFET)—Chad Young, UT Dallas
4:50–5:10 p.m.  4.3 Constant Shape Factor Frequency-Modulated Charge Pumping (FMCP)—Jason Ryan, Jason Campbell, Jibin Zou, Kin Cheung, Jason Campbell, John Conley, Oregon State University
5:10–5:30 p.m.  4.4 (LATE) Fast-Capacitance for Advanced Device Characterization—Pragya Shrestha, Kin Cheung, Jason Campbell, Jason Ryan, National Institute of Standards and Technology, Helmut Baumgart, Old Dominion University
6:00–7:30 p.m.  DINNER, (Dining Room)
7:30–9:00 p.m.  Poster Session (Cathedral Room), Chair: Jason Ryan, NIST
9:00–10:00 p.m.  Mixer

TUESDAY, October 15
7:00–8:00 a.m.  BREAKFAST (Dining Room)
8:00–8:05 a.m.  Announcements (Angora Room)
8:05–9:10 a.m.  Tutorial #2: Reliability and Parasitic Effects of GaN HEMTs—Matteo Meneghini, University of Padova

Session #5: (Angora Room) III/V Device Reliability
9:10–9:45 a.m.  5.1 (INVITED) Investigating the High-k/InGaAs MOS System for Future Logic Applications—Paul Hurley, Tyndall National Inst.
9:45–10:20 a.m.  5.2 (INVITED) Assessment of GaN High-Electron-Mobility Transistor Reliability for RF Amplifier Applications—David J. Meyer, Naval Research Lab
10:20–10:40 a.m.  Coffee Break
10:40–11:15 a.m.  5.3 (INVITED) Modeling Reliability of GaN HEMTs—Dragica Vasileska, Arizona State University
11:15–11:35 a.m.  5.4 (LATE) RF Reliability of Gate Last InGaAs nMOSFETs with High-k Dielectric—Guntrade Roll, Mikael Egard, Sofia Johansson, Lars Ohlsson, Lars-Erik Wernersson, Erik Lind, Electrical and Information Technology, Lund University
11:35–12:00 p.m.  Group Picture
12:00–1:00 p.m.  LUNCH, (Dining Room)
1:00–2:05 p.m.  Tutorial #3: Assessing the Quality & Reliability of CMOS Image Sensors Through Image Statistics—Daniel Van Blerkom, Forza Silicon Corporation
Session #6 (Angora Room)  Circuit /Products
2:05–2:40 p.m.  6.1 (INVITED) Device Degradation Models for Circuit Reliability Simulation—Guido Sasse, NXP Semiconductors
2:40–3:15 p.m.  6.2 (INVITED) CMOS IC Reliability Assessment for Government Applications—Michael Fritze, University of Southern California
3:15–3:35 p.m.  Coffee Break
3:35–4:10 p.m.  6.3 (INVITED) Reliability Testing and Test Structure Design in an Age of Increasing Complexity—William McMahon, Globalfoundries
4:10–4:30 p.m.  6.4 Defect-Based Compact Model for Circuit Reliability Simulation in Advanced CMOS Technologies—Ivan Sanchez Esqueda, University of Southern California, Hugh Barnaby, Arizona State University
4:30–4:50 p.m.  6.5 (LATE) Circuit Relevant Well Charging from Metal Antenna and its Degradation on Digital MOS Transistor Reliability—Andreas Martin, Infineon Technologies AG

Session #7 (Angora Room)  Memory
4:50–5:25 p.m.  7.1 (INVITED) Understanding Operation and Reliability in HfOx RRAM Devices through Physical Modeling—Luca Larcher, University of Modena
5:25–5:45 p.m.  7.2 Dependence of Maximum RESET Current on the Duration of Current Overshoot—Pragya Shrestha, David Nminibapiel, Jason Campbell, Kin Cheung, NIST, Helmut Baumgart, Old Dominion University, Shweta Deora, Gennadi Bersuker, SEMATECH
5:45–6:05 p.m.  7.3 Comparison of Reliability of Single and Stacked high-k Structures of Charge Trapping Memories—Chongwang Sun, Liyang Pan, Zhigang Zhang, Lifang Liu, Institute of Microelectronics, Tsinghua University
6:05–7:30 p.m.  DINNER, (Dining Room)
7:30–9:00 p.m.  Discussion Groups: Chair: Wayne Ellis, Rambus

SIGs: Chair: Wayne Ellis, Rambus
9:00–10:00 p.m.  SIGs: (90 minute parallel sessions for each topic) Attendees are to participate in one of the groups

WEDNESDAY, October 16
7:00–8:00 a.m.  BREAKFAST (Dining Room)
8:00–8:05 a.m.  Announcements, (Angora Room)
8:05–9:10 a.m.  Tutorial #4: Taking the Closest Look Possible: Atomistic Modeling of Reliability Problems—Franz Schanovsky, TU Wien

Session #8 (Angora Room)  Bias Temperature Instability / Hot Carriers – I
9:10–9:45 a.m.  8.1 (INVITED) A Novel Strategy for Ideal MOS Stack of High Dielectric Reliability: Preventing Leakiness of the Thatched Roof to keep the Tatami Comfortable—Ziyuan Liu, Renesas Electronics
9:45–10:05 a.m.  8.2 Relevance of Non-exponential Single-defect-induced Threshold Voltage Shifts for NBTI Variability—Jacopo Franco, Ben Kaczer, Philippe J. Roussel, Maria Toledano-Luque, Pieter Weckx, imec, Tibor Grasser, TU Wien
10:05–10:25 a.m.  8.3 Drift Compensating Effect during Hot-Carrier Degradation of 130nm Dual Gate Oxide p-channel Transistors—Gunnar Rott, Heiko Nielen, Hans Reisinger, Wolfgang Gustin, Infineon Technologies AG, Stanislav Tyaginov, Tibor Grasser, TU Wien
10:25–10:45 a.m.  Coffee Break
10:45–11:05 a.m.  8.4 Experimental Analysis of Defect Nature and Localization under Hot-Carrier and Bias Temperature Damage in Advanced CMOS Nodes—Wafa Arfaoui, Xavier Federspiel, STMicroelectronics, Alain Bravaix, ISEN – IM2NP, Pascal Mora, Mustapha Rafik, David Roy, STMicroelectronics
11:05–11:25 a.m.  8.5 A Unified Model for AC Bias Temperature Instability—Gilson Wirth, UFRGS, Jacopo Franco, Ben Kaczer, IMEC
11:25–11:45 a.m.  8.6 Zero/Low Field SDR and SDT used for Atomic Scale Probes of NBTI and TDDB—Corey Cochrane, Patrick Lenahan, University of Modena
11:45–12:05 p.m.  8.7 Unusual Bias Temperature Instability in SiC DMOSFET—Zakariae Chbili, Kin Cheung, Jason Campbell, John Suehle, National Institute of Standards and Technology, Dimitris Ioannou, George Mason University, Sei-Hyung Ryu, CREE, Aivars Lelis, Army Research Laboratory
12:05–1:30 p.m.  LUNCH (Dining Room) Take out Lunch bags available
1:30–6:00 p.m.  Open The afternoon is free for discussion, hiking & other recreation. All attendees are required to be back before darkness.
6:00–7:30 p.m.  DINNER, (Dining Room)
7:30–8:30 p.m.  Poster Session (Cathedral Room),  Chair: Jason Ryan, NIST
8:30–9:30 p.m.  Discussion Groups: Chair: Wayne Ellis, Rambus (90 minute parallel sessions for each topic) Attendees are to participate in one DG

THURSDAY, October 17
7:00–8:00 a.m.  BREAKFAST (Dining Room)
8:00–8:05 a.m.  Announcements, (Angora Room)
8:05–9:10 a.m.  Tutorial #5: Electromigration in Pb-free Interconnect—Minhua Lu, IBM T. J. Watson Research Center
9:10–10:15 a.m.  Tutorial #6: Cracking Resistant of Interconnect Structures for Advanced Microelectronics—Tom Shaw, IBM T. J. Watson Research Center
10:15–10:40 a.m.  Break / Check out

Session #9 (Angora Room)  Bias Temperature Instability / Hot Carriers – II
10:40–11:00 a.m.  9.1 (LATE) Reliability and Performance Considerations for NMOSFET Pass Gates in FPGA Applications—Ben Kaczer, imec, Chris Chen, Jeff Watt, Kaushik Chanda, Altera Corporation, Pieter Weckx, Maria Toledano Luque, Guido Groeseneken, imec, Tibor Grasser, TU Wien
11:00–11:20 a.m.  9.2 (LATE) Essential Ingredients for Modeling of Hot-Carrier Degradation in Ultra-Scaled MOSFETs—Stanislav Tyaginov, Markus Bina, Jacopo Franco*, Dmitri Osintsev, Yannick Wimmer, Ben Kaczer*, Tibor Grasser, TU Wien, *imec
11:20–12:00 p.m.  DG Summary/SIG Report/Wrap-up
12:00–1:00 p.m.  LUNCH, (Dining Room) & then the Workshop Ends—Attendees must leave the Stanford Sierra Camp