2015 IEEE International Integrated Reliability Workshop

PROGRAM SCHEDULE

SUNDAY, October 11 Please have lunch before arriving at the camp; no lunch will be served at the camp.

3:00-6:00 p.m. Registration: Pick up badges and handout Discussion Group and SIG Signup (*Lodge Lounge*)

3:00-8:00 p.m. Lodge check-in. Get room assignment (prearranged) & room key. (If physically challenged please notify desk of special needs.)

6:00-7:30 p.m. DINNER (*Dining Room*)

7:30-8:30 p.m. **Sunday Night Tutorial** (*Angora Room*) Planes—Jim Lloyd, SUNY-Poly

8:30-10:00 p.m. Social (*Old Lodge*)

MONDAY, October 12

7:00-8:00 a.m. BREAKFAST (*Dining Room*)

Plenary Session (*Angora Room*)

8:00-8:10 a.m. Welcome & Introduction—General Chair: Jason Ryan, NIST

8:10-8:20 a.m. Technical Program Overview—Richard Southwick, IBM

8:20-9:20 a.m. **Keynote:** Reliability of Handheld Consumer Devices—Prasad Chaparala, Amazon

Session #1 (*Angora Room*) — **Special Topics,** Chair: Tom Kopley, Fairchild

9:20-9:50 a.m. 1.1 **(INVITED)** Engineering the Performance of MIM Tunnel Diodes and Capacitors with ALD Nanolaminate Bilayer Insulators—John Conley, Oregon State University

9:50-10:20 a.m. 1.2 **(INVITED)** Defect Limited Reliability and Transport in Carbon Nanotube and Graphene Devices—David Estrada, Boise State

10:20-10:50 a.m. Coffee and Snack Break

10:50-11:55 a.m. **Tutorial # 1:** AgELESS: Aging Estimation and Lifetime Enhancement in Silicon Systems—Sachin Sapatnekar, Univ. of Minnesota

12:00-1:00 p.m. LUNCH (*Dining Room*)

1:00-2:05 p.m. **Tutorial # 2:** Ionizing Radiation Effects in Electronic Devices with an Emphasis on Non- volatile Memories—Marta Bagatin, Univ. of Padova

Session #2 (*Angora Room*) **— Non-volatile Memories,** Chair: Andreas Aal, Volkswagen

2:05-2:35 p.m. 2.1 **(INVITED)** Solid-State-Drive (SSD) Qualification and Reliability Strategy—Todd Marquart, Micron

2:35-3:05 p.m. 2.2 **(INVITED)** Reliability challenges in resistive switching memories technology—Shweta Deora, Sematech

3:05-3:35 p.m. Coffee and Snack Break

3:35-4:00 p.m. 2.3 Investigation of the reliability degradation of scaled SONOS memory transistors—Johannes Ocker, NaMLab gGmbH

4:00-4:25 p.m. 2.4 Advanced test vehicle for in-depth RRAM nanosecond-range switching-time resolution and reliability assessment—Clément Nguyen, CEA-LETI

Session #3 (*Angora Room*) **— Random Telegraph Noise,** Chair: Jason Campbell, NIST

4:25-4:55 p.m. 3.1 **(INVITED)** Defect-centric perspective for combined RTN and BTI time-dependent variability—Pieter Weckx, IMEC

4:55-5:20 p.m. 3.2 Further Understandings on Impacts of La incorporation in HfSiON/TiN nFETs Through Comprehensive Random Telegraph Noise Characterizations—Jiezhi Chen, Toshiba

5:20-5:30 p.m. Discussion Group Overview (*Angora Room*)

5:30-6:00 p.m. Poster Setup (*Cathedral Room*), Chair: Andreas Aal, Volkswagen; Vice-Chair Jim Lloyd, SUNY-Poly

6:00-7:30 p.m. DINNER (*Dining Room*)

7:30-9:00 p.m. **Poster Session** (*Cathedral Room*), Chair: Andreas Aal, Volkswagen; Vice-Chair Jim Lloyd, SUNY-Poly

9:00-10:00 p.m. Social (*Old Lodge*)

TUESDAY, October 13

7:00-8:00 a.m. BREAKFAST (*Dining Room*)

8:00-8:05 a.m. Announcements (*Angora Room*)

8:05-9:10 a.m. **Tutorial #3:** Modeling of Hot-carrier Degradation in GaN Transistors—Yevgeniy S. Puzyrev, Vanderbilt

Session #4 (*Angora Room*) **— Late News Part 1,** Chair Jim Lloyd, SUNY-Poly

9:10-9:35 a.m. 4.1 **(LATE NEWS)** Effect of Dielectric Thickness and Annealing on Threshold Voltage Instability of Low Temperature Deposited High-k Oxides on ZnO TFTs—Chadwin Young, Univ. of Texas at Dallas

9:35-10:05 a.m. Coffee and Snack Break

Session #5 (*Angora Room*) **— III-V,** Chair: Richard Southwick, III

10:05-11:25 a.m. 5.1 **(INVITED)** Oxide defects and their Effect on Reliability of III-V and Ge high K gate stacks—John Robertson, Cambridge

10:35-11:00 a.m. 5.2 Charge Feedback Mechanisms at Forward Threshold Voltage Stress in GaN/AlGaN HEMTs—Alexander Grill, TU Wien
11:00-11:25 a.m. 5.3 Extraction of interface and border traps in beyond-Si devices by accounting for generation and recombination in the semiconductor—Gabriele Sereni, Univ. of Modena

11:25-12:00 p.m. Group Picture (*Flag Pole*)

12:00-1:00 p.m. LUNCH (*Dining Room*)

Session #6 (*Angora Room*) **— BEOL,** Chair: Tom Shaw, IBM

1:00-1:30 p.m. 6.1 **(INVITED)** A sampling approach for efficient BEOL TDDB assessment—Andrew Kim, IBM

1:30-2:35 p.m. **Tutorial #4:** FinFET Reliability—Suresh Uppal, Globalfoundries

Session #7 (*Angora Room*) **— Si MOSFET Reliability,** Chair: Christian Schlünder, Infineon

2:35-3:05 p.m. 7.1 **(INVITED)** Aging Model Challenges in Tri-gate Technologies—Stephen Ramey, Intel
3:05-3:35 p.m. 7.2 **(INVITED)** Reliability Aging and Modeling of Chip Package Interaction on Logic Technologies Featuring High-k Metal Gate Planar and FinFET Transistors—Jen-Hao Lee, TSMC

3:35-4:05 p.m. Coffee and Snack Break

4:05-4:35 p.m. 7.3 **(INVITED)** From WLR to Product Reliability and Qualifications in the 3D Transistor Era—Sangwoo Pae, Samsung
4:35-5:00 p.m. 7.4 Novel Charge Pumping Method Applied to Tri-Gate MOSFETs for Reliability Characterization—Brad Bittel, Intel
5:00-5:25 p.m. 7.5 Consideration of Relxation Effect on Voltage Ramp Stress Measurement in CMOS Reliability—Dong-Hwi Lee, Inha Univ.

6:00-7:30 p.m. DINNER (*Dining Room*)

7:30-8:30 p.m. **Discussion Groups:** Chair: Bill McMahon, Globalfoundries and Matt Hogan, Mentor (60 minute parallel sessions for each topic.) Attendees are to participate in one of the groups.

8:30-10:00 p.m. Social (*Old Lodge*)

WEDNESDAY, October 14

7:00-8:00 a.m. BREAKFAST (*Dining Room*)

8:00-8:05 a.m. Announcements (*Angora Room*)

8:05-9:10 a.m. **Tutorial #5:** Modeling and Characterization of Hot-Carrier Stress Degradation in Power MOSFETs—Susanna Reggiani, Univ. of Bologna

Session #8 (*Angora Room*) **— Large statistics,** Chair: Brad Bittel, Intel

9:10-9:35 a.m. 8.1 Advanced MOSFET variability and reliability characterization array—Marko Simicic, KU Leuven / IMEC
9:35-10:00 a.m. 8.2 Wafer Level Test Arrays with Simple BIST to Expedite Process Development for Circuit Reliability—Ming-Han Hsieh, TSMC
10:00-10:25 a.m. 8.3 Influence of MOSFET geometry on the statistical distribution of NBTI induced parameter degradation—Christian Schlünder, Infineon

10:25-10:55 a.m. Coffee and Snack Break

10:55-11:20 a.m. 8.4 Comparison of recoverable and permanent NBTI component variability—Damien Nouguier, STMicro
11:20-11:45 a.m. 8.5 Massively Parallel TDDB testing : SiC Power devices—Zakariae Chbili, NIST (currently at Globalfoundries)

12:00-1:00 p.m. LUNCH (*Dining Room*)

1:00-6:00 p.m. Open The afternoon is free for discussion, hiking & other recreation. All attendees are required to be back before darkness.

6:00-7:30 p.m. DINNER (*Dining Room*)

7:30-8:30 p.m. **Poster Session** (*Cathedral Room*), Chair: Andreas Aal, Volkswagen; Vice-Chair Jim Lloyd, SUNY-Poly

8:30-9:30 p.m. **Discussion Groups:** Chair: Bill McMahon, Globalfoundries and Matt Hogan, Mentor (60 minute parallel sessions for each topic.) Attendees are to participate in one of the groups.

THURSDAY, October 15

7:00-8:00 a.m. BREAKFAST (*Dining Room*)

8:00-8:05 a.m. Announcements (*Angora Room*)

8:05-9:10 a.m. **Tutorial #6:** Nanoscopic techniques for studying dielectric breakdown and switching induced morphological changes and defects—K.L. Pey, Singapore Univ. of Tech. and Design

9:10-9:40 a.m. **(INVITED)** Electron Devices Society: Activities and Opportunities—Samar Saha, IEEE EDS

9:40-10:10 a.m. Coffee and Snack Break / Check Out of Room

Session #9 (*Angora Room*) **— Late News Part 2,** Chair: Jim Lloyd, SUNY-Poly

10:10-10:35 a.m. 9.1 **(LATE NEWS)** Smart-array for pipelined BTI characterization—Vamsi Putcha, IMEC
10:35-11:00 a.m. 9.2 **(LATE NEWS)** Field-Induced Generation of Electron Traps in the Tunnel Oxide of Flash Memory Cells—Yuri Tkachev, Silicon Storage Tech.

11:00-11:40 a.m. **DG Summary / SIG Report / Wrap-up**

11:40-12:00 p.m. Fill out and return survey

12:00-1:00 p.m. LUNCH (*Dining Room*) & then the Workshop Ends—Attendees must leave the Stanford Sierra Camp

Poster Presentations (not including Walk-in Posters)

Refereed Posters

RP01 STUDY OF THE IMPACT OF DIELECTRIC AGING ON COPLANAR WAVEGUIDE PERFORMANCE —A.P. Nguyen, U. Luders , and F. Voiron (IPDIA)

RP02 COMPARISON OF RANDOM TELEGRAPH NOISE, ENDURANCE AND RELIABILITY IN AMORPHOUS AND CRYSTALLINE HAFNIA-BASED RERAM—K. Beckmann, J. Holt, N. Cady, (SUNY Polytechnic Institute, CNSE), and J. Nostrand (Air Force Research Laboratory)

RP03 POLY RESISTOR DEGRADATION-MODELING AND MECHANISM—S. Jayanarayanan (Maxim Integrated)

RP04 THE STRENGTH OF BEOL STRUCTURES FABRICATED USING LOW K MATERIALS AND ITS IMPACT ON CPI FAILURES—T. Shaw, E. Misra, D. Questad, X. Liu, G. Bonilla, T. Wassick, S. Hosadurga, K. Smith, G. Osborne, D. Kioussis, J. Wright, R. Bisson, I. Paquin, M. Lamorey, R. Bouchard, S. Tetreault, D. Stone, C. Muzzy, B. Sundlof, and T. Daubenspeck (IBM)

RP05 RELAXATION-FREE CHARACTERIZATION OF FLASH PROGRAMMING DYNAMICS ALONG P-E CYCLING—J. Coignus, A. Vernhet (CEA-LETI), G. Torrente, S. Renard, D. Roy (STMicroelectronics), and G. Reimbold (CEA-LETI)

RP06 USING THE CHARGE PUMPING GEOMETRIC COMPONENT TO EXTRACT NBTI INDUCED MOBILITY DEGRADATION—M. Boubaaya, H. Tahi, C. Tahanout, and B. Djezzar (Centre de Developpement des Technologies Avancees, CDTA)

RP07 CHARGE-BASED STOCHASTIC AGING ANALYSIS OF CMOS CIRCUITS—T. Hillebrand, N. Hellwege, N. Heidmann, S. Paul, and D. Peters-Drolshagen (Institute of Electrodynamics and Microelectronic, University of Bremen)

RP08 MEMORY YIELD AND LIFETIME ESTIMATION CONSIDERING AGING ERRORS—D-H Kim and L. S. Milor (Georgia Institute of Technology)

RP09 HOT CARRIER STRESS MODELING: FROM DEGRADATION KINETICS TO TRAP DISTRIBUTION EVOLUTION—G. Torrente, X. Federspielf, D. Rideau, F. Monsieur, C. Tavernier (STMicroelectronics), J. Coignus (CEA-LETI), D. Roy (STMicroelectronics) and G. Ghibaudo (IMEP-LAHC)

RP10 TOTAL DOSE RADIATION AND ENDURANCE COMBINED CHARACTERIZATION OF TAOX-BASED COMMERCIAL RERAM—J. Yang-Scharlotta, M. Amrbar (JPL), J. Holt (SUNY Polytechnic Institute), and D. Sheldon (JPL)

RP11 COMBINED VRAMP AND TDDB ANALYSIS FOR GATE OXIDE RELIABILITY ASSESSMENT AND SCREENING—T. Kopley, M. Ring, C. Choi, and J. Colbath (Fairchild Semiconductor)

RP12 ON THE TEMPERATURE BEHAVIOR OF HOT-CARRIER DEGRADATION—S. Tyaginov, M. Jech, P. Sharma (TU Wien), J. Franco, B. Kaczer (IMEC), T. Grasser (TU Wien)

Open Posters

OP01 NBTI STRESS ON POWER VDMOS TRANSISTORS UNDER LOW MAGNETIC FIELD—C. Tahanout, M. Boubaaya (Centre de Developpement des Technologies Avancees, CDTA), M. Marah, and B. Nadji (Universit de M'hamd Bougara, Boumardes, UMBB)

OP02 EFFECTS OF BIAS TEMPERATURE STRESS ON THE NEGATIVE MAGNETORESISTANCE OF SICOH—B. McGowan (SUNY Polytechnic Institute), A. Kennedy (Fairfield University), W. Nolting, and J. Lloyd (SUNY Polytechnic Institute)

OP03 PROCESS RELIABILITY SIMULATION—T. Turner (Texas Semicon Labs)

OP04 RADIATION TESTING OF TANTALUM OXIDE-BASED RESISTIVE MEMORY—J. Holt (SUNY Polytechnic Institute), J. Yang-Scharlotta (JPL), and N. Cady (SUNY Polytechnic Institute)