The IEEE International Integrated Reliability Workshop (IIRW) focuses on ensuring electronic device reliability through fabrication, design, testing, characterization, and simulation, as well as identification of the defects and physical mechanisms responsible for reliability problems.

**October 9-13, 2016**

**Stanford Sierra Conference Center**

Fallen Leaf Lake, CA, USA

**Abstract Deadline**

July 11, 2016

**Late News Deadline**

August 22, 2016

**General Chair:**

Ricki Southwick

IBM, USA

**TPC Chair:**

Tom Kopley

Fairchild, USA

**www.iirw.org**

**Outstanding features** of the IIRW are

- Strong plenary, invited, and tutorial presentations
- Strong technical program (platform and posters)
- Unparalleled opportunities to meet world-leading experts
- Discussion and special interest groups
- Unique rustic and secluded environment

**IIRW 2016** invites abstracts related to the reliability of

- Gate/Interconnect dielectrics (SiO₂, SiON, high-k, low-k)
- Conventional and emerging memory devices (RRAM, etc.)
- CMOS, non-CMOS (III-V), and novel devices
- MEMS and other sensors
- Transistor reliability (hot carriers, NBTI/PBTI, TDDB)
- Defects
- Modeling and simulation of reliability issues
- Interconnects
- Impact of transistor degradation on circuit reliability
- Design-in reliability (products, circuits, systems, processes)
- Customer/manufacturer product reliability requirements
- Wafer level reliability tests
- Single event upsets and irradiation related reliability issues

Your two page abstract should state clearly and concisely the results of your work and why they are significant. Representative data and figures that support your proposal are REQUIRED.

For more information please visit www.iirw.org, or contact the technical program chair:

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