2001 International Integrated Reliability Workshop

Stanford Sierra Camp, S. Lake Tahoe, CA

October 15-18, 2001 http://www.irps.org/irw/

IEEE/Integrated Reliability Workshop
P.O. Box 308
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General Chair
Andreas Martin
Infineon Technologies AG
49-89-234-45257...fax...-45822
Andreas.Martin@infineon.com

Technical Program Chair
Linda M. Head
Rowan University
856-256-5335...fax...-5241
email: head@rowan.edu

Technical Program Vice Chair
Gennadi Bersuker
International SEMATECH
512-356-7045...fax...891-0277
gennadi.bersuker@sematech.org

Tutorial & Registration Chair
Al Strong
IBM MicroElectronic
email: astrong@us.ibm.com

DG/Sig's Chair
Prasad Chaparala
National Semiconductor
prasad.chaparala@nsc.com

Poster Sessions Chair
Emmanuel Vincent
STMicroelectronics
emmanuel.vincent@st.com

Poster Sessions Vice Chair
Bui Nguyen
Lattice Semiconductor Corp.

Finance Chair
Nels A. Dumin
Texas Instruments
email: nels.dumin@ti.com

Finance Vice Chair
Yuan Chen
Lucent Technologies
chenyuan@lucent.com

Arrangements Chair
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Infineon Technologies
rolf.vollertsen@infineon.com

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jconley@sharplabs.com

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kiami.rogers@infineon.com

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NIST
email: john.suehle@nist.gov

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PROGRAM ANNOUNCEMENT!

Workshop Experience

You are cordially invited to participate in the 2001 Integrated Reliability Workshop. It provides a unique environment for envisioning, developing, and sharing reliability technology for present and future semiconductor applications. Here you will closely interact with your peers at moderated discussion groups, open poster sessions, technical presentations, and special interest groups. All Workshop activities take place in a relaxed and rustic setting that promotes an atmosphere of interactive learning and knowledge sharing. You should come away from the workshop intellectually refreshed!

'01 Workshop Features:

- ✶ **Keynote:** ***Can Praseodymium Oxide be an Alternative High-K Gate Dielectric ?*** **Hans-Joachim Müssig & Hans-Jörg Osten, IHP, Frankfurt, Germany**
- ✶ **Group Discussions**
  - WLR and EM
  - Oxides
- ✶ **Tutorials**
  - Ultra-thin Gate Oxide Reliability
  - Full-Chip Reliability Simulation
  - Atomic Scale Defects
  - Trap Generation Phenomenons
  - Plasma Charging Damage
  - Plasma Charging Effects
- ✶ **15+ Technical Presentations on:**
  - Customer Product Reliability Requirements
  - Reliability of Ultra-Thin Oxides
  - Contributors to Failure
  - Wafer Level Reliability
- ✶ **Three IEEE Training Videos:**
  - Oxide Wearout/Breakdown/Reliability
  - MEMS Performance & Reliability
  - Accelerated Stress Testing
- ✶ **Refereed/Open Poster Sessions**
- ✶ **Special Interest Groups**

Major Technical Themes

As industry retools and regroups for the coming technology sector expansion, it is crucial that the reliability of new materials, devices and products be kept at the forefront of development and design. The Integrated Reliability Workshop is focused this year on exactly this mission.

On Monday afternoon, we are leading our program this year with tutorials on two diverse but important topics in materials and product reliability, "*Ultra-thin Gate Oxide Reliability: Past and Present Trends in Characterization, Physical Modeling, and Assessment*," by Eric M. Vogel from the Semiconductor Electronics Division at NIST, and "*Full-Chip Reliability Simulation for VDSM Integrated Circuits*," by Zhihong Liu, President and CEO of Celestry Design Technologies, Inc.

New this year are ***four additional tutorials*** interspersed with oral presentation sessions, which include "late-breaking news" presentations on high performance BiCMOS SiGe reliability and on Cu/low-k process reliability issues. On Tuesday, one tutorial is by P.M. Lenahan of The Pennsylvania State University on "*Atomic Scale Defects Involved in MOS Reliability Problems*," another is "*Plasma Charging Damage - Mechanisms, Measurements and Solutions*" by James P. McVittie from Stanford University. On Wednesday, another pair of tutorials will be given: "*Trap Generation Phenomenon in Thin Dielectrics Under Electrical Stress*" by Gennadi Bersuker from International SEMATECH; and "*Plasma Charging Effects on ULSI Technology Reliability*" by Nguyen D. Bui from Lattice Semiconductor Corporation.

Our ***keynote*** picks up on another important theme, reliability of novel materials. It is "Can praseodymium oxide be an alternative high-k gate dielectric material for silicon integrated circuits?" by Hans-Joachim Müssig and Hans-Jörg Osten from IHP in Frankfurt (Oder), Germany.

As usual, we will have ample time for one-on-one exchanges, organized discussion groups, our popular and productive SIGs (Special Interest Groups) and poster sessions where all our attendees are encouraged to display a poster with their most recent work, ideas, and results. As a very special feature, attendees can view three recent IEEE sponsored ***training videos***: "Oxide Wearout/Breakdown/Reliability," "MEMS Performance & Reliability", and "Accelerated Stress Testing." To purchase these videos would be quite costly for your organization, but IRW attendees can view them free of charge at the Workshop.

Tell your colleagues about the workshop! They need to attend.

Tell your manager! You and your organization cannot afford to miss this investment in learning to help you deal with today and to prepare for tomorrow.

–over–

KEYNOTE

Can Praseodymium Oxide be an Alternative High-*K* Gate Dielectric Material for Silicon Integrated Circuits? – *Hans-Joachim Müssig and Hans-Jörg Osten, IHP, Im Technologiepark 25, D-15236 Frankfurt (Oder), Germany*

Scaling of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs beyond 100 nm) requires the thickness of present, SiO_2-based gate dielectrics to approach 1.5 nm. The device design will be constrained by an unacceptably high leakage current due to electrons tunneling directly through the ultra-thin SiO_2 layer. The challenge is the replacement of the traditional silicon dioxide gate dielectric by new materials with higher dielectric constants (*K*).

We show that crystalline praseodymium oxide films of the Pr_2O_3-type grown on Si(001) have outstanding dielectric properties, displaying a dielectric constant of around 30 (independent of substrate doping), very low leakage current density ($5{\times}10^{-9}$ A/cm^2 at $V_g = \pm 1.0$ V @ EOT = 1.4 nm), good reliability, and reversible electrical breakdown. We report on the structure and stability of thin praseodymium oxide layers on Si(001) by combining Scanning Tunneling Microscopy (STM), X-ray Photoelectron Spectroscopy (XPS), and Auger Electron Spectroscopy (AES). We present experimental evidence and theoretical explanations based on *ab initio* pseudopotential simulations for the transition of PrO_2 into Pr_2O_3, and the formation of an ultra-thin Si-O interlayer between Pr_2O_3 and the Si substrate.

TUTORIALS

Chair: Alvin Strong, IBM

Ultra-thin Gate Oxide Reliability: Past and Present Trends in Characterization, Physical Modeling, and Assessment, *Eric M. Vogel, Semiconductor Elect. Div., NIST*

Tutorial #1 Monday, 1:30–3:30 p.m. *(Angora Room)*

Recently, the reliability of gate oxides has become a critical concern as oxide thickness is scaled below 3 nm in advanced technologies. It has been proposed that the fundamental limit to further device scaling is the intrinsic reliability of the gate dielectric. An overview of past and present thin oxide reliability characterization techniques and wear-out physics will be presented. Special emphasis will be placed on issues relating to the characterization and understanding of breakdown in present-technology, ultra-thin gate oxides where excessive tunneling currents and soft breakdown complicate reliability assessment.

Full-Chip Reliability Simulation for VDSM Integrated Circuits, *Zhihong Liu, Ph.D. President and CEO, Celestry Design Technologies, Inc.*

Tutorial #2, Monday, 4:00–6:00 p.m. *(Angora Room)*

As the transistor channel length scales down toward 0.1 micron and new processes loom ahead, circuit reliability simulation technologies should be on the finger-tips of the circuit designers to maximize design performance by minimizing design guard-band, to speed up design closure by reducing design iterations, and to ensure long-term circuit reliability. Most common circuit reliability issues such as hot-carrier effects and electromigration are discussed in this tutorial with emphasis on the full-chip design flow, as an alternative to the more popular TD fix of those issues. It has been shown that in the era of VDSM and in the emergence of more advanced processes such as SOI, thin dielectric films and copper interconnects, more degradation mechanisms need to be investigated and more complicated modeling issues need to be solved in the simulation procedure. Both full-chip transistor-level and cell-based solutions should be provided for circuit designers with million-transistor/million-gate capacity and Spice-accuracy. Reliability simulation constitutes one of the key roles in the silicon-accuracy sign-off flow for full-chip designs, as well as parasitic extraction, coupling noise timing analysis, and power grid IR drop.

Atomic Scale Defects Involved in MOS Reliability Problems, *P.M. Lenahan, The Pennsylvania State University*

Tutorial #3, Tuesday, 1:20–3:20 p.m. *(Angora Room)*

Many reliability problems in metal-oxide-silicon (MOS) technology have been quite carefully and extensively characterized in a purely “electronic” sense. However, quite sophisticated “electronic” characterization has not always been accompanied by even a rudimentary understanding of the atomic scale defects involved. Such an understanding would be useful in building-in reliability. [1]

A fundamental understanding of the imperfections involved in many MOS reliability problems has developed in recent years, in large part via magnetic resonance studies. [2] Although imperfect and incomplete, there now exists a rudimentary understanding of the several defects which dominate Si/SiO_2 interface trap generation, oxide deep levels involved in stress induced leakage currents, and (in thicker oxides) charge trapping.

In this presentation, I’ll explain how magnetic resonance measurement techniques have been applied to metal-insulator-silicon systems and summarize what we know about the structure and electronic properties of the most important of the more than a dozen electronic defects identified to date. The presentation will focus on defects involved in oxide leakage currents and Si/SiO_2 interface instabilities. Other trapping centers in oxides, nitrides, oxynitrides, and BPSG interlevel dielectrics will be reviewed.

References:

[1]. H.A. Schafft, D.L. Erhart, and W.K. Gladden, Microelectron. Reliab. 37, 3 (1997)

[2]. P.M. Lenahan and J.F. Conley, Jr., J.Vac. Sci. Technol. B. 16, 2134 (1998)

Plasma Charging Damage - Mechanisms, Measurements and Solutions, *James P. McVittie, Allen Center for Integrated Systems, Stanford University*

Tutorial #4, Tuesday, 1:20–3:20 p.m. *(Cathedral Room)*

This tutorial will give an overview of plasma charging problems during wafer fabrication. It will start with an introduction to plasmas and go on to show how charging can occur and result in device damage. Direct plasma measurements and charging monitoring will be reviewed. An overview of device damage measurements will be given. Methods for eliminating this type of damaged will be discussed along with the impact of going to thinner dielectrics and SOI structures.

Trap Generation Phenomenon in Thin Dielectrics Under Electical Stress, *Gennadi Bersuker, International SEMATECH*

Tutorial #5, Wed., 10:00–12:00 a.m. *(Cathedral Room)*

1. Introduction: What is a dielectric: from the physicist’s description to the EE’s one - nature of chemical bonds and band gap, interface w/ metals/semiconductors, band offset, electron energy barrier, FN equation.
2. Simulations of oxide structure
3. Physical analysis of oxides: defects
4. Selected electrical results
5. Overview of oxide trap generation models: requirements/limitations

Plasma Charging Effects on ULSI Technology Reliability, *Nguyen D. Bui, Technology Development Group, Lattice Semiconductor Corp.*

Tutorial #6, Wed., 10:00–12:00 a.m. *(Angora Room)*

Plasma charging induced damage has become a well-known issue in advanced technology. The problem requires a solution that may involve many disciplines of the semiconductor industry such as semiconductor equipment, process development, technology integration, and chip design. As the technologies continue to scale, the damage could become a reliability hazard. The plasma process has been used with increased frequency in advanced technologies, thus leading to the potential for severe plasma process-induced damage. We must learn to minimize plasma process-induced damage on the semiconductor device in both front-end and back-end modules of the process technology. In this tutorial, the charging damage mechanism will be discussed briefly. Damage detection, structure

(continued on back of registration form)

2001 *International*

INTEGRATED RELIABILITY WORKSHOP

PRELIMINARY PROGRAM

MONDAY, October 15

1:00 – 8:00 p.m. Lodge check-in. Get room assignment (prearranged), room key, lodge area map, and information. (if physically challenged please notify desk of special needs)

1:00 – 6:00 p.m. Registration (*Dining Room Lounge*): Pick up badges & handout. Signup for Discussion Groups and SIGs.

1:30 – 3:30 p.m. Tutorial #1: "Ultra-thin Gate Oxide Reliability: Past and Present Trends in Characterization, Physical Modeling, and Assessment", *Eric M. Vogel, Semiconductor Electronics Division, NIST*

3:30 – 4:00 p.m. Break

4:00 – 6:00 p.m. Tutorial #2: "Full-Chip Reliability Simulation for VDSM Integrated Circuits", *Zhihong Liu, Ph.D. President and CEO, Celestry Design Technologies, Inc*

6:15 – 7:30 p.m. DINNER *(Dining Room)*: Speakers dine with your Session Chair.

7:30 – 8:00 p.m. Signup for Discussion Groups & SIGs (*Dining Room Lounge*); Poster Preparation (*Old Lodge*)

8:00 – 10:30 p.m. Mixer & Poster Session *(Cathedral Room)*

TUESDAY, October 16

7:00 – 8:00 a.m. BREAKFAST *(Dining Room)*

8:15 – 8:30 a.m. Welcome & Introduction: Andreas Martin, General Chair & Technical Program Overview: Linda Head, Tech. Prog. Chair *(Angora Room)*

8:30 – 9:30 a.m. Keynote: "Can Praseodymium Oxide be an Alternative High-k Gate Dielectric Material for Silicon Integrated Circuits?" – *Hans-Joachim Müssig and Hans-Jörg Osten*, *IHP, Frankfurt(Oder), Germany*

9:30 – 10:00 a.m. Break

10:00 – 11:40 a.m. Session #1: Reliability of Ultra-Thin Oxides (RUO), Chair: Eric Vogel, NIST

- RUO-1 "Preliminary Investigation of Hafnium Oxide Deposited via Atomic Layer Chemical Vapor Deposition (ALCVD)", J.F. Conley, Jr., Y. Ono, D.J. Tweet, W. Zhuang, Sharp Laboratories of America and M. Khaiser, R. Solanki, Oregon Graduate Institute
- RUO-2 "Latent Reliability Degradation of Ultra Thin Oxides After Heavy Ion and Gamma-Ray Irradiation", B. Wang, J.B. Bernstein, University of Maryland, J.S. Suehle, Eric Vogel, Semiconductor Electronics Division NIST, J.F. Conley, Jr., NASA Jet Propulsion Laboratories (Currently, Sharp Labs of America), A.H. Johnston, North Carolina State University
- RUO-3 "Oxide Thickness Dependence of Time to Breakdown and Voltage to Breakdown for Ultra Thin Oxides (Tox < 32 Å)", F. Monsieur, E. Vincent, D. Roy, S. Bruyere, STMicroelectronics, G. Pananakakis, G. Ghibaudo, LPCS/ENSERG
- RUO-4 "Accurate and Efficient Design of Experiment for Ultra Thin Oxide Reliability Assessment. Application to a 20 Å Gate Oxide.", F. Monsieur, E. Vincent, D. Roy, S. Bruyere, STMicroelectronics, G. Pananakakis, G. Ghibaudo, LPCS/ENSERG

11:40 – 12:10 p.m. Group Picture

12:10 – 1:20 p.m. LUNCH *(Dining Room)*

1:20 – 3:20 p.m. Tutorial 3 & 4 in parallel:

- Tutorial 3: "Atomic Scale Defects Involved in MOS Reliability Problems", *P.M. Lenahan, The Pennsylvania State University*
- Tutorial 4: "Plasma Charging Damage - Mechanisms, Measurements and Solutions, *James P. McVittie, Allen Center for Integrated Systems, Stanford University*

3:20 – 4:00 p.m. Break

4:00 – 5:40 p.m. Session #2 Customer Product Reliability Requirements (CPR), Chairs: Gennadi Bersuker, Int'l SEMATECH & Abdullah Yassine, AMD

- CPR-1 "Model to Predict Reliability of ONO Non-Volatile Memory", Santosh Kumar, Edmund Russell, Cypress Semiconductor
- CPR-2 "Stress Induced MOSFET Mismatch for Analog Circuits", Yuan Chen, J. Zhou, F. Hui, A.S. Oates, Agere Systems
- CPR-3 "Hot Carrier Reliability and Design of N-LDMOS Transistor Arrays", Douglas Brisbin, A. Strachan, P. Chaparala, National Semiconductor Corp.
- CPR-4 "Contribution of Gate Induced Drain Leakage to Overall Leakage and Yield Loss in Digital Submicron VLSI Circuits", Oleg Semenov, M. Sachdev University of Waterloo, A. Pradzynski, Gennum Corp.

6:00 – 7:30 p.m. DINNER *(Dining Room)*

7:30 – 9:00 p.m. Discussion Groups: Chair: Prasad Chaparala, National Semiconductor Corp. (90 minute parallel sessions for each topic) Attendees are to participate in one group: 1) WLR and EM or 2) Oxides

9:00 – 10:30 p.m. Individual SIG Meetings (To be announced at the Camp.)

WEDNESDAY, October 17

7:00 – 8:00 a.m. BREAKFAST *(Dinning Room)*

8:00 – 8:15 a.m. Announcements *(Angora Room)*

8:15 – 9:45 a.m. Session #3 Contributors to Failure (CTF), Chair: Andreas Martin, Infineon Technologies

- CTF-1 "Positive/Negative BT Instability in Scaled N/P-MOSFETs and MOSCs", Hisao Katto, Science University of Tokyo
- CTF-2 "A New Observation in Hot-Carrier Induced Drain Current Degradation in 0.18 µm nMOSFETs", Jone F. Chen, Chih-Pin Tsao, National Cheng Kung University
- CTF-3 "New Insights of Boron Penetration on Dual Gate Oxide with Different Thickness", Owen Wang, B. Lin, S. Lin, MOSEL VITELIC, INC.

9:45– 10:00 a.m. Break

10:00 – 12:00 pm Tutorial 5 & 6 in parallel:

Tutorial 5: "Trap Generation Phenomenon in Thin Dielectrics Under Electical Stress", *Gennadi Bersuker, International SEMATECH*	Tutorial 6: "Plasma Charging Effects on ULSI Technology Reliability", *Nguyen D. Bui, Technology Development Group, Lattice Semiconductor Corp.*

12:00 – 1:30 p.m. LUNCH *(Dining Room)*: Take out Lunch bags available.
1:30 – 4:30 p.m. Open The afternoon is free for discussion, hiking & other recreation; or for viewing training videos, shown in parallel:
(1) Oxide Wearout/Breakdown/Reliability, Dave Dumin (Clemson University) (*Angora Room*);
(2) MEMS Performance and Reliability, Paul McWhorter, Bill Miller, and Sam Miller (Sandia National Labs) *(Cathedral Rm);*
(3) Accelerated Stress Testing, T. Paul Parker (Lucent Technologies), H. Anthony Chan (AT&T Labs.), Charles Felkins (Storage Technology), and Anthony Oates (Lucent Technologies).
4:30 – 6:00 p.m. Mixer & Poster Session *(Cathedral Room)*

6:00 – 7:30 p.m. DINNER *(Dining Room)*

7:30 – 9:00 p.m. Discussion Groups: Chair: Prasad Chaparala, National Semiconductor Corp.
(90 minute parallel sessions for each topic)
Attendees are to participate in one group: 1) WLR and EM or 2) Oxides

9:00 – 10:30 p.m. Individual SIG Meetings

THURSDAY, October 18

7:00 – 8:00 a.m. BREAKFAST (*Dining Room*)

8:15 – 8:30 a.m. Announcements *(Angora Room)*

8:30 – 11:00 p.m. Session #4 Wafer Level Reliability (WLR), Chair: Emmanuel Vincent, STMicroelectronics

WLR-1 "Isothermal EM Test Development of CU/Oxide Single Damascene Interconnect", Andrew Yap (Kin Leong), Chartered Semiconductor Manufacturing
WLR-2 "WLR Monitoring Methodology for Assessing Charging Damage on Oxides Thicker than 3nm Using Antenna Structures", David Smeets, A. Martin, J. Fazekas, Infineon Technologies AG
WLR-3 "Relationship Between TDDB Testing and Wafer Level Ramped QBD Testing Using Both Fixed Current and Current Density Stressing", Ed Mullen, C. Leveugle, J. Molyneaux, Analog Devices, J. Prendergast, National Institute of Technology, Ireland, J.S. Suehle, NIST
LBP-1 "Electromigration Current Limits of High Speed SiGe Bipolar Transistors Influenced by Device Self-Heating", Kevin Brelsford, Jae-Sung Rieh, Ping-Chuan Wang, and Greg Freeman, IBM SiGe Custom Logic
LBP-2 "Wafer Level Testing of Inter-line Dielectrics in Copper/low-k Structures", G. B. Alers, G. Harm, T. Suwwan de Felipe, Novellus

11:00 – 12:00 p.m. Wrap-Up

12:00 – 1:30 p.m. LUNCH *(Dining Room)*—Leave the Stanford Sierra Camp after lunch unless you are attending JC14.2

2:00 p.m. JEDEC 14.2, Committee on Wafer Level Reliability Meeting

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2001 IRW REGISTRATION FORM (Use also for reserving accommodations to EIA/JEDEC Committee JC14.2 meeting, Oct. 18-19)

(Please type, print or attach business card)

Meeting registration automatically includes a room reservation.

NAME: ______________________ TITLE: ____________
Last First Initial

COMPANY: ______________________________
Mail Stop

ADDRESS: ______________________________

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City State/Country Zip/Postal Code

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ADVANCE REGISTRATION FEES

IEEE Member ____________ **$945*** ________
(member No. Req'd)

NON-IEEE Member .... **$995*** ________

** Includes workshop attendance & handout materials, tutorial attendance, 3 nights lodging (Monday—Wednesday) 9 meals (dinner Monday—lunch Thursday), Final Workshop Report.*

EXTRA COPIES of Workshop Final Report ....Qty: ______ x **$80** ________

JC-14.2 Mtg. accommodations** **$180** ________

*** Includes 1 night lodging (Thursday), 3 meals (dinner Thursday— lunch Friday)*

TOTAL REMITTED $ ________

Cancellation fees: $50 after Sept. 21 ; full fee after Oct. 5

Send this completed form and payment to:
IRW Registration; P.O. Box 308; Westmoreland, NY 13490

Paying by credit card... fax to 315-336-9134
Questions? becky@sar101.com or 315-339-3968
or web site: http://www.irps.org/irw
Wire Transfer (add $30 for bank fees) call for details

Tahoe Casino Express: The Tahoe Casino Express **runs from Reno to Tahoe** between 6 a.m. and midnight with departures from Reno at: 6:15 a.m., 8:15 a.m., 9:15, 10:15, 11:15, 12:15 p.m., 1:15, 2:15, 3:15, 5:30, 7:30, 9:30, and 12:30 a.m. The Express costs $17 each way ($30 round trip) and tickets can be purchased at the Express counter located in the baggage area in the Reno airport. Travel time is approximately 1½ hours. The Casino Express can be reached at 800-446-6128. The Express **leaves the Horizon Casino at Lake Tahoe and returns to Reno** on the following schedule: 4:10 a.m., 6:10, 8:10, 9:10, 10:10, 11:10, 12:10 p.m., 1:10, 2:10, 3:10, 4:10, 5:10, 7:25, and 10:25 p.m. Tickets may be purchased in the Horizon Casino at the main cashier's cage. For more information check http://www.tahoecasinoexpress.com.

Stanford Sierra Camp offers courtesy transportation for conference attendees from the Horizon Casino between 10 a.m. and 10 p.m. on Registration Day (Monday, Oct. 15). Return trips to the Casino are offered on the last day of the conference only. If you are planning on using the Casino Express, please notify Stanford Sierra Camp (530-541-1244) at least ONE WEEK prior to your arrival date. If you find yourself stranded, please call the camp at the same number. The IRW Arrangements Committee may be able to provide emergency service to and from the casino.

TUTORIALS *(continued from page 2)*

design, and common industrial damage detection devices will be reviewed. Plasma-charging damage protection devices and evaluation methods will be discussed. The plasma-charging damage effect on logic, non-volatile memories, and RF circuits will be discussed briefly.

DISCUSSION GROUPS

Chair: Prasad Chaparala, National Semiconductor Corp.

The evening discussion group program is regarded as a favorite highlight of the workshop experience. Attendees will have a choice of two areas on Tuesday and Wednesday evenings. The topics to be discussed will be at the discretion of those participating in the group. Each group is assigned a pair of leaders who have extensive experience with the area and will help to guide the discussion. Everyone is encouraged to bring along data and/or ideas to share on topics that are of particular interest. As we get closer to the date of the workshop, we will be surveying registered attendees so that we may prepare relevant discussion outlines to be distributed at the camp. This year's discussion areas and leaders are:

1. WLR and EM:
   Harry Schafft (NIST) and
   Emmanuel Vincent (ST Microelectronics)
2. Oxides:
   John Conley (SharpLabs) and
   Eric Vogel (NIST)

SPECIAL INTEREST GROUPS

Chair: Prasad Chaparala, National Semiconductor Corp.

The Special Interest Groups (SIGs) program at the Workshop has been very successful in fostering collaborative work on important reliability issues and we look forward to continuing growth and renewal in our SIGs. The formation of SIGs is encouraged as a natural extension of the Discussion Group sessions. Anyone interested in more information on SIGs see http://www.irps.org/irw/sig/.

REFEREED & OPEN POSTER SESSIONS

(Monday & Wednesday Evening)

Chair: Emmanuel Vincent, ST Microelectroonics

All attendees have the opportunity to present a poster to communicate and discuss their ideas and newest results on technical projects or issues. Please indicate on the registration form your intention to bring a poster by reserving a poster display board (32" × 40" or 81 cm × 100 cm) in the space provided. Your work should be in Landscape format on 8½ × 11" or A4 paper with a maximum of twelve pages. In addition, you are invited to submit a two-page abstract of your poster presentation for inclusion in the Workshop Final Report. See www.irps.org/irw/poster/ for details and deadlines. This is a great opportunity for you to obtain useful feedback about your work and to test your ideas with your peers. If you are presenting a refereed or invited poster, a display board will be reserved for you.

JEDEC 14.2 Meeting. The JEDEC 14.2, Wafer Level Reliability Standards Committee, meeting will be held immediately after the Workshop at the Stanford Sierra Camp on Thursday afternoon and continued on Friday morning. Members, alternates, and guests are welcome. The cost for the accommodations is $180.00, which includes Thursday night dinner and lodging *and* Friday breakfast and lunch. All attendees must leave the camp after lunch on Friday. If you have any questions or if you want to become a member of JC-14.2, please call the JEDEC office at (703) 907-7558 or www.jedec.org, or call Mike Dion, JC-14.2 Chair at (407) 724-7067.

More Information. We expect an exciting workshop again this year. We look forward to your active participation in the many Workshop activities and your valuable contribution to the technical discussions. If you have additional questions, please contact either: the Technical Program Chair, Linda Head, by phone, 856-256-5335, fax…5241, or email: head@rowan.edu; the Tech. Prog. Vice Chair, Gennadi Bersuker, by phone 512-356-7045, fax ...891-0277, email: gennadi.bersuker@sematech.org; or the General Chair, Andreas Martin, by phone, ++49 89 234 45257; fax ...45822; or e-mail: Andreas.Martin@Infineon.com. Web site: www.irps.org/irw.

REGISTER NOW!

Complete and send in the enclosed registration form. Please register early. We have sold out in past years. Space at the Camp limits IRW to roughly 120 attendees.

We look forward to seeing you at the Workshop!

Sincerely,

Linda Head
Technical Program Chair

RESPONSIBILITIES OF ATTENDEES

You are expected to come prepared to participate actively in the discussions and meetings by sharing your experiences, concerns, questions, views, technical information, and test data, as appropriate. Your active involvement in the formal, as well as in the informal meetings and activities, is the key ingredient for maximizing the value of the workshop for you and your fellow attendees.

ACCOMMODATIONS

The Stanford Sierra Camp provides an ideal setting for the workshop. The isolated location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees. Clusters of 2 and 3 bedroom cabins are nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake. Please note; while each attendee is assigned a bedroom, bathroom facilities within each cabin are shared. Towels and soap are provided. All rooms have decks with magnificent views of Fallen Leaf Lake and surrounding Sierra peaks.

- **All participants must stay at the camp during the workshop.**
- **We cannot accommodate spouses or any companions at the camp**.
- **Accommodations are *not* available at the Stanford Camp for any day before or after the workshop.**
- Smoking is permitted outdoors only. Smoking is not be permitted in the sleeping or meeting rooms.
- Arrangements can be made for those with special dietary or physical requirements. Please send your requirements with the registration or call 315-339-3968.
- A message board will be available for incoming calls, (530) 541-1244. There are pay telephones for outgoing calls. There are no telephones in the rooms.

ARRANGEMENTS INFORMATION

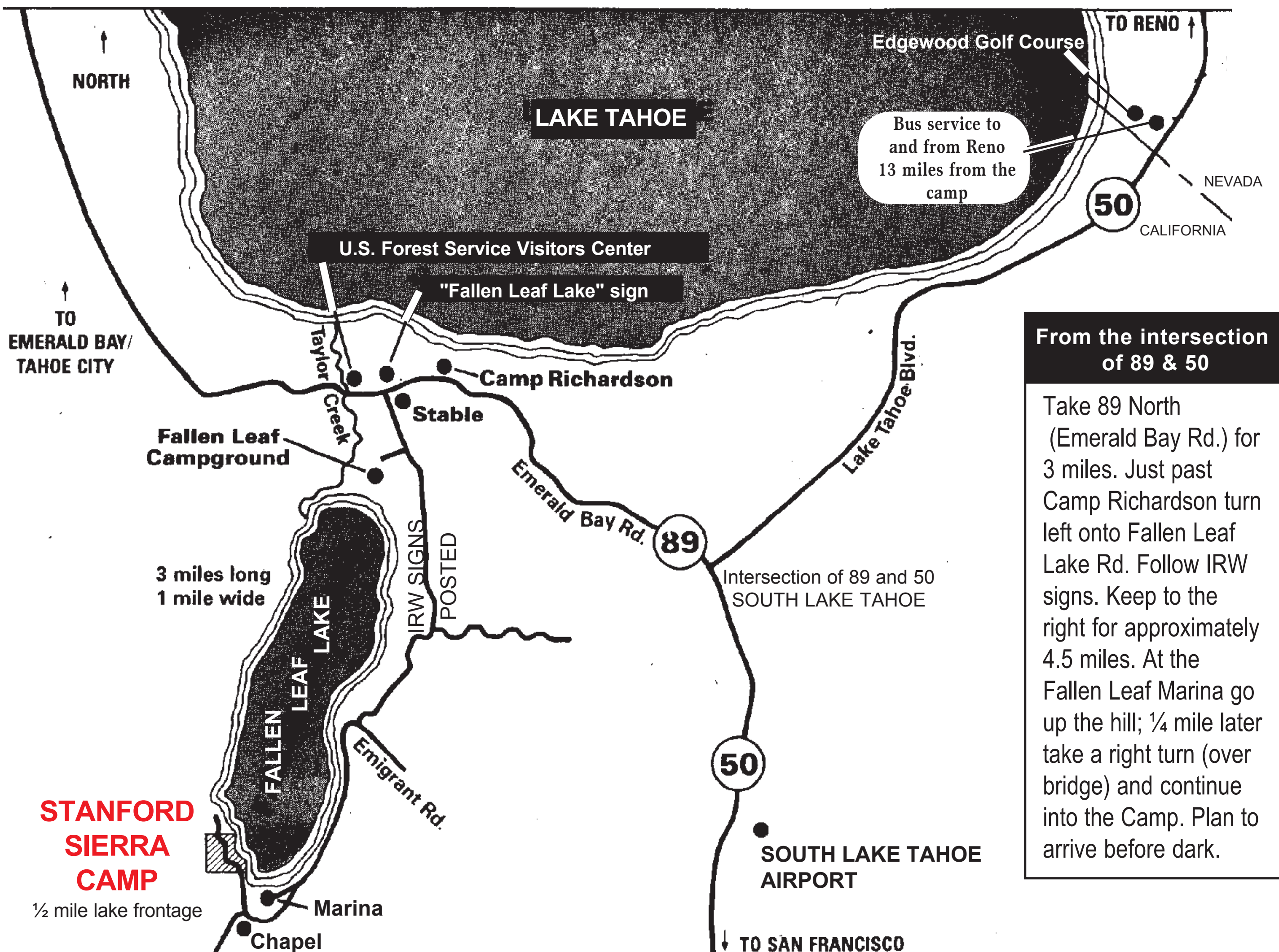
Special discounted airfares for IRW have been negotiated by IEEE Global Travel Services. Please note that this service can be used by attendees traveling from within or outside of the United States and Canada. Discounts are as high as 20% off the lowest published airfares with American, TWA, Continental and United airlines. Special rates have also been negotiated with Avis Rental Car Company. Travel arrangements using the negotiated air carriers or the carriers of your choice can be made through IEEE Global Travel Services by calling between the hours of 8:30 a.m. and 5:30 p.m. EST. Monday through Friday. Within the US and Canada, call 800-879-4333; and outside of the US and Canada, call +1 732-562-5387. Or, visit their on-line travel service web site at www.ieeetravelonline.org. At this secure site you can search, reserve, and ticket your travel anytime, anywhere. You may also fax your requirements to the IEEE Global Travel Services at 732-562-8815. When faxing, please be sure to include your travel dates, departure, return times, phone and fax numbers and mention the IEEE IRW. A Travel Counselor will contact you promptly.

TRANSPORTATION NOTE: The Stanford Sierra Camp is located on Fallen Leaf Lake, a few miles from South Lake Tahoe. The nearest major airport is the Reno International Airport. Reno is approximately two hours from the Stanford Sierra Camp. Currently no commercial flights are available to the South Lake Tahoe Airport.

- Transportation is available from Reno International Airport to the South Lake Tahoe terminus at Horizons Casino via the ***Tahoe Casino Expres***s. For ***Tahoe Casino Express*** schedule details see back of this page, call 800-446-6128, or check http://www.tahoecasinoexpress.com.

WHAT TO BRING

It may be cold or warm at 6000 feet in the Sierra in October. We recommend that you bring warm clothing and a coat. Comfortable, informal dress is encouraged. No suits, ties, or high heels please. You may want to bring hiking shoes. There are numerous outstanding hiking trails around the camp. A small flashlight would be helpful to find your cabin after dark.



From the intersection of 89 & 50

Take 89 North (Emerald Bay Rd.) for 3 miles. Just past Camp Richardson turn left onto Fallen Leaf Lake Rd. Follow IRW signs. Keep to the right for approximately 4.5 miles. At the Fallen Leaf Marina go up the hill; ¼ mile later take a right turn (over bridge) and continue into the Camp. Plan to arrive before dark.