2006 IEEE International
Integrated Reliability Workshop

http://www.iirw.org

October 16-19, 2006
Stanford Sierra Camp, Lake Tahoe, CA

CALL FOR PAPERS

The International Integrated Reliability Workshop focuses on ensuring semiconductor reliability through fabrication, design, testing, characterization, and simulation, as well as identification of the defects and physical mechanisms responsible for reliability problems. Through tutorials, discussion groups, special interest groups, and the informal format of the technical program, a unique environment is provided for understanding, developing, and sharing reliability technology for present and future semiconductor applications as well as ample opportunity for discussions and interactions with colleagues.

Hot reliability topics for the workshop include: high-κ and nitrided SiO_2 gate dielectrics, NBTI, Cu interconnects and low-κ dielectrics, product reliability and burn-in strategy, impact of transistor degradation on circuit reliability, reliability modeling and simulation, SiGe and strained Si, III-V, SOI, optoelectronics, single event upsets, and reliability assessment of novel devices and future "nano"-technologies.

We invite you to submit a presentation proposal that addresses any integrated semiconductor related reliability issue, including the following topics:

- Designing-in reliability (products, circuits, systems, processes):
  methodologies and concepts, modeling and simulation tools, reliability-driven design rules and checkers, use of WLR and/or reliability test structures for design rule verification, in-line detection and reliability analysis.
- Customer product reliability requirements / manufacturer reliability tasks:
  limits to achieving future reliability targets, reliability evaluation methodologies and reporting systems, data bases, chip reliability, product reliability extrapolation to use conditions, wafer and package burn-in, packaging, strategies to eliminate burn-in, correlation between process, yield, and reliability, qualification strategies.
- Root cause defects, physical mechanisms, and simulations
  nature of defects, physical and electrical characterization of defects, defect generation models, process induced defects and degradation, modeling/simulation of reliability related circuit constraints, accelerated testing and lifetime extrapolation.
- Identification and characterization of reliability effects:
  failure mechanisms in new materials and device structures, reliability aspects of: high-k gate stack, Cu interconnects and low-k dielectrics, MOS and bipolar transistors including FinFETs and 3D gates, SiGe and strained Si, SOI, MEMS devices, optoelectronics, high voltage devices, unique reliability phenomena and failure mechanisms in Non-Volatile memories, new memory technologies, MRAM, nanotechnology reliability assessment, and limits to accelerated stressing.
- Deep sub-micron transistor and circuit reliability:
  single event effects and soft errors, ESD, electromigration, mechanical stress related issues, hot carrier effects, NBTI, dielectric breakdown, reliability extrapolation, impact of new material systems, modeling and simulation, impact of scaling,
- Wafer level reliability tests, test approaches, and reliability test structures:
  fast stress tests and analysis methodologies, reduction in development time, in-line monitors, relation to circuit-element and package-level tests, use and interpretation of WLR data, success stories, fine tuning of WLR implementation, accounting for censoring, design, characterization, and data analysis for chip or package level circuit-like structures (including electrical and/or physical test/analysis).

PAPER AND POSTER SUBMISSION INSTRUCTIONS

Abstract Submission Deadline: ***July 14, 2006***

Your *two page extended abstract* (maximum two pages) should state clearly and concisely the results of your work and why they are significant. Representative data and figures that support your proposal are REQUIRED.

Please e-mail your abstract to the Technical Program Chair *either as an MS Word document or .pdf attachment*. Fax submissions will NOT be accepted. A separate cover page must include your full business address, i.e., author name, affiliation, address, telephone and fax numbers, and the e-mail address for each co-author. State whether *oral or poster* presentation is

preferred. All submissions will be acknowledged by email within one week. If you do not receive acknowledgment of your submission by that time, please contact the Technical Program Chair.

Viewgraphs for all accepted oral presentations are required by September 8, 2006 for inclusion in the Presentation Handout that is distributed at the workshop. A written version of your presentation is due at the workshop for inclusion in the Final Report.

The workshop offers the opportunity for expanded versions of selected workshop manuscripts to be part of a special IIRW Proceedings Issue of the IEEE Transactions in Device and Material Reliability (TDMR) in June 2007.

Late paper Submission: A limited number of late breaking news manuscripts (maximum four pages) will be considered and may be submitted until September 5, 2006. Accepted late papers will be included in the Final Report.

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LODGING & FACILITIES

Nestled throughout the pines and cedars along the shoreline of Fallen Leaf Lake, a few miles from South Lake Tahoe, are clusters of 2 and 3 bedroom cabins furnished in the rustic style of an alpine resort. Each cabin is equipped with shared bathroom facilities. All rooms have decks with magnificent views of Fallen Leaf Lake and the surrounding Sierra peaks. The physical isolation of the location and the absence of distractions, such as in-room phones and television sets, encourages extensive interaction among the Workshop attendees.

Lodging will be provided only to registered attendees of IIRW. In accordance with housing rules, no guests of the attendees are allowed.

HISTORY

The Wafer Level Reliability Workshop was initiated in 1982 through the efforts of O. D. "Bud" Trapp, of Technology Associates, and the financial support of DARPA (Defense Advanced Research Projects Agency) to foster the approach of introducing reliability characterizations at the wafer level. Also involved were The Stanford University Integrated Circuits Laboratory and the University of California, Berkley, Dept. of Electrical Engineering and Computer Sciences. Financial support by DARPA continued for the first eight years of the workshop. Bud Trapp was able to continue the operation of the workshop only until early 1992 when he asked Harry Schafft (then the new Chair of the IRPS Board of Directors) to assume responsibility for the workshop. With fellow IRPS Board member Pat Kennedy to lead the arrangements and operation of the workshop, a Technical Advisory Committee to represent the interests of the reliability community, and the oversight of IRPS, the workshop was transformed, within two years, into a self-sustaining technical meeting with IEEE sponsorship. In 1993, the name of the workshop was changed to the Integrated Reliability Workshop to reflect the importance of integrating the approach of building-in reliability in the design, processing, and manufacture of semiconductor products.

SPONSORS

The International Integrated Reliability Workshop is sponsored by

the IEEE Electron Device Society

and

the IEEE Reliability Society,

and in doing so the IIRW Final Report is published by IEEE and archived.

MORE INFORMATION

For more information, please see our web-page: http://www.iirw.org