**SUNDAY, October 14**  Please have lunch before arriving at the camp; no lunch will be served at the camp.

3:00–6:00 p.m.  Registration: Pick up badges & handout (Lodge Lounge)

3:00–8:00 p.m.  Lodge check-in. Get room assignment (prearranged) & room key.  
(If physically challenged please notify desk of special needs.)

6:15–7:30 p.m.  DINNER, (Dining Room) authors; dine with your session chair

7:30–9:30 p.m.  **Invited Talk:** DNA Nanotechnology – Nanophotonic Device & Medical Applications—William Knowlton, Boise State Univ.

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**MONDAY, October 15**

7:00–8:00 a.m.  BREAKFAST (Dining Room)

8:05–8:20 a.m.  (Angora Room) Welcome & Introduction: Drew Turner, General Chair; Technical Program Overview: Jason Campbell, TP Chair

8:20–9:20 a.m.  **Keynote:** Device Reliability Physics: Past, Present, and Future—James Stathis, IBM

9:25–10:30 a.m.  Tutorial #1: Making Memristors a Reality: Advances in Physical Understanding and Device Integration—Janice Nickel, HP Labs

10:30–10:45 a.m.  Break

10:45–11:55 a.m.  **Session #1: Resistive Memory I,** Chair: Jason Campbell, NIST (Angora Room)

1.1 (INVITED) Challenges in Engineering RRAM Technology for High Density Applications—Nirmal Ramaswamy, Micron

1.2 (INVITED) Origin of Conductive Filaments and Resistive Switching in HfO₂-based RRAMs—Gennadi Bersuker, SEMATECH

12:00–1:00 p.m.  LUNCH, (Dining Room)

1:00–3:10 p.m.  **Session #2: Resistive Memory II,** Chair: Jason Campbell, NIST (Angora Room)

2.1 (INVITED) Reliability of Low Current Filamentary HfO₂ RRAM Discussed in the Framework of the Hourglass SET/RESET Model—Robin Degraeve, IMEC

2.2 (INVITED) Physical Modeling of Voltage-Driven Resistive Switching in Oxide RRAM—Daniele Ielmini, Politecnico di Milano

2.3 (INVITED) Resistive Switching Random Access Memory - Materials, Device, Interconnects, and Scaling Considerations—Yi Wu, Stanford University

2.4 Effect of Crystallinity on Endurance and Switching Behavior of HfOₓ-based Resistive Memory Devices—Jihan Capulong, Benjamin Briggs, Seann Bishop, Michael Hovish, Richard Matyi, Nathaniel Cady, University at Albany

3:10–3:25 p.m.  Break

3:25–4:35 p.m.  **Session #3: Advanced Gate Stack**—Jason Ryan, NIST

3.1 (INVITED) III-V Nanoelectronics for Logic Applications—Suman Datta, Penn State University

3.2 (INVITED) Semiconductor Equipment Requirements for Ge and III-V CMOS—Khaled Ahmed, Intermolecular

4:35–5:40 p.m.  **Tutorial #2:** Vehicle Reliability Field Data Analysis - Best Practise at Mercedes-Benz Cars—Matthias Grabert, Daimler AG

5:45–7:00 p.m.  DINNER, (Dining Room)

7:00–8:30 p.m.  Poster Session (Cathedral Room), Chair: Jason Ryan, NIST

8:30–10:00 p.m.  Mixer

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**TUESDAY, October 16**

7:00–8:00 a.m.  BREAKFAST (Dining Room)

8:05–8:15 a.m.  Announcements (Angora Room)

8:15–9:20 a.m.  **Tutorial #3:** Reliability Aspects of GaN-Based Power Devices for High Voltage Switching Applications—Joachim Würfl, Ferdinand-Braun-Institut

9:20–10:30 a.m.  **Session #4: Circuit / Product Reliability,** Chair: Richard Southwick, IBM (Angora Room)

4.1 (INVITED) Ensuring System Reliability: From FET Characterization to Performance Prediction—Aditya Bansal, IBM

4.2 (INVITED) Uncovering Circuit Reliability Effects Using Dedicated On-Chip Monitors—Chris H. Kim, Univ. of Minnesota

10:30–10:45 a.m.  Break

10:45–11:45 a.m.  4.3 (INVITED) Product/Device Reliability Correlations for Low-Power Applications—Sriram Kalpat, Qualcomm


11:45–12:15 p.m.  Group Picture

12:15–1:15 p.m.  LUNCH, Dining Room

1:15–2:20 p.m.  **Tutorial #4:** BeOL Reliability—Tim Sullivan, IBM

2:20–3:20 p.m.  **Session #5: BeOL Reliability,** Chair: Barry O’Connell, Fairchild Semiconductor (Angora Room)

5.1 (INVITED) Reliability of Low-k Interconnect Dielectrics—Gaddi Haase, Sandia National Labs

5.2 Reliability Investigations of Down-stream Copper Interconnect with Different Tungsten-VIA Structures—An-Shun Teng, Ronnie Tu, Robyn Chen, Ming-Yi Lee, Allen Dai, Shih-Chin Lee, Thomas Wen, Chih-Yuan Lu, Macronix

3:20–3:35 p.m.  Break

3:35–4:00 p.m.  5.3 Through Silicon Via impact on above BeOl Time Dependent Dielectric Breakdown—Thomas Frank, Emmanuel Chery, Cedrick Chappaz, Lucile Amaud*, Lorena Anghel*, STMicroelectronics, *CEA-Leti, *TIMA Laboratory

4:00–5:05 p.m.  **Tutorial #5:** Main Reliability Challenges with Copper TSV’s—Kristof Croes, IMEC
5:05–5:55 p.m. **Session #6: Methods/FLASH**, Chair: Jason Ryan, NIST (Angora Room)
6.1 Zero-Field Spin Dependent Transport in the Absence of an Oscillating Magnetic Field: A Means to Study Reliability Based Defects in Fully Processed Devices—Corey Cochrane and Patrick Lenahan, Penn State University
6.2 Characterization of Cell to Cell Interference in TANOS NAND Flash Memory—Byeong-In Choe and Jong-Ho Lee, Seoul National University
6:00–7:30 p.m. **DINNER**, (Dining Room)
7:30–9:00 p.m. **Discussion Groups**: Chair: James Wu, PMC-Sierra (90 min in parallel) Attendees are to participate in one of the groups
   • Resistive Memories – Advancement and Future
   • FEOL Reliability – General Discussion
9:00–10:00 p.m. **SIGs**: Chair: James Wu, PMC-Sierra

**WEDNESDAY, October 17**
7:00–8:00 a.m. **BREAKFAST** (Dining Room)
8:00–8:05 a.m. Announcements, (Angora Room)
8:05–9:10 a.m. **Tutorial #6**: Modeling of Hot-carrier Degradation: Physics & Controversial Issues—Stanislav Tyaginov, Technical University of Vienna
9:10–10:35 a.m. **Session #7: Bias Temperature Instability**, Chair: Tibor Grasser, TU Wien (Angora Room)
   7.1 (INVITED) NBTI and Dynamic Variability in Highly-Scaled Planar and Gate-All-Around MOSFETs—Ru Huang, Peking University
   7.2 Recent Results Concerning the Influence of Hydrogen on the Bias Temperature Instability—Gregor Pobegen, Michael Nelhiebel, Tibor Grasser*, KAI, *Technical University of Vienna
   10:30–10:45 a.m. Break
10:45–12:00 p.m. **Session #8: PID/Transistor**, Chair: Pat Lenahan, Penn State University (Angora Room)
   8.1 (INVITED) High-k MOSFET Performance Degradation by Plasma Process-Induced Charging Damage—Koji Eriguchi, Kyoto University
   8.2 On the Impact of the Layout of MOSFET test-structures on the NBTT-, PBTI- and HCS-lifetime due to PID—Christian Schluender and Andreas Martin, Infineon
   8.3 Optimized Data Assessment for Hot Carrier and Fowler-Nordheim Stresses on Thick MOS Gate Oxides with Plasma Process Induced Charging Damage—Andreas Martin and Andreas Koten, Infineon
   8.4 OFF-State induced \( V_{th} \) relaxation after PBTI Stress—Steve Kupke, Steve Knebel, Guntrade Roll, Stefan Slesazeck, Gernot Krause*, Gottfried Kurz*, Thomas Mikolajick, NaMLab, *GLOBALFOUNDRIES
   8.5 Comparison between Gateoxide Lifetime Models with Rseries and Trapping Effect Correction in the FN-Regime—Andreas Aal, University of Duisburg-Essen
12:00–1:30 p.m. **LUNCH** (Dining Room — Take out Lunch bags available)
1:30–6:00 p.m. Open The afternoon is free for discussion, hiking & other recreation. All attendees are required to be back before darkness.
6:00–7:30 p.m. **DINNER**, (Dining Room)
7:30–8:30 p.m. **Poster Session** (Cathedral Room), Chair: Jason Ryan, NIST
8:30–10:00 p.m. **Discussion Groups**: Chair: James Wu, PMC-Sierra (90 min in parallel) Attendees are to participate in one of the groups
   • Extrinsic Breakdown Characteristics – How to avoid them – How to detect them ?
   • Product/Circuit Reliability – From FET modeling to Zero Field Failure
   • BEOL Reliability – General Discussion
   • Additional DG session by demand/interest – contact DG chair

**THURSDAY, October 18**
7:00–8:00 a.m. **BREAKFAST** (Dining Room)
8:00–8:05 a.m. Announcements, (Angora Room)
8:05–10:20 a.m. **Session #9: III-V Devices**, Chair: Drew Turner (Angora Room)
   9.1 Reverse Bias Stress Test of GaN HEMTs for High-Voltage Switching Applications—Michael Dammann, Heiko Czap, Joachim Rüster, Fraunhofer
   9.2 HBT Reliability Modeling Strategy for RF and mmW Applications—Salim Ighilahriz, Florian Cacho, Vincent Huard, Laurence Moquillon, Philippe Benech*, Jean-Michel Fournier*, STMicroelectronics, *IMEP-LHAC
10:20–10:45 a.m. Break / Check out
10:45–11:35 a.m. **Session #10: PID/Transistor**, Chair: Pat Lenahan, Penn State University (Angora Room)
   10.1 (INVITED) High-k MOSFET Performance Degradation by Plasma Process-Induced Charging Damage—Koji Eriguchi, Kyoto University
   10.2 On the Impact of the Layout of MOSFET test-structures on the NBTT-, PBTI- and HCS-lifetime due to PID—Christian Schluender and Andreas Martin, Infineon
   10.3 Optimized Data Assessment for Hot Carrier and Fowler-Nordheim Stresses on Thick MOS Gate Oxides with Plasma Process Induced Charging Damage—Andreas Martin and Andreas Koten, Infineon
   10.4 OFF-State induced \( V_{th} \) relaxation after PBTI Stress—Steve Kupke, Steve Knebel, Guntrade Roll, Stefan Slesazeck, Gernot Krause*, Gottfried Kurz*, Thomas Mikolajick, NaMLab, *GLOBALFOUNDRIES
   10.5 Comparison between Gateoxide Lifetime Models with Rseries and Trapping Effect Correction in the FN-Regime—Andreas Aal, University of Duisburg-Essen
10:20–10:45 a.m. Break / Check out
10:45–11:35 a.m. **Session #9: III-V Devices**, Chair: Drew Turner (Angora Room)
   9.1 Reverse Bias Stress Test of GaN HEMTs for High-Voltage Switching Applications—Michael Dammann, Heiko Czap, Joachim Rüster, Fraunhofer
   9.2 HBT Reliability Modeling Strategy for RF and mmW Applications—Salim Ighilahriz, Florian Cacho, Vincent Huard, Laurence Moquillon, Philippe Benech*, Jean-Michel Fournier*, STMicroelectronics, *IMEP-LHAC
11:35–12:00 p.m. **DG Summary/SIG Report/Wrap-up**
12:00–1:00 p.m. **LUNCH**, (Dining Room) & then the Workshop Ends—Attendees must leave the Stanford Sierra Camp